TPS61021A 3-A Boost Converter with 0.5-V Ultra Low Input Voltage

1 Features

- Input Voltage Range: 0.5 V to 4.4 V
- 0.9 V Minimum Input Voltage for Startup
- Output Voltage Setting Range: 1.8 V to 4.0 V
- 91% Efficiency at V_{IN} = 2.4 V, V_{OUT} = 3.3 V and I_{OUT} = 1.5 A
- 2.0-MHz Switching Frequency
- I_{OUT} > 1.5 A at V_{OUT} = 3.3 V when V_{IN} > 1.8 V
- 17-µA Typical Quiescent Current
- ±2.5% Reference Voltage Accuracy over -40°C to 125°C
- PFM Operation Mode at Light Load
- True Disconnection Between Input and Output During Shutdown
- Output Over Voltage Protection
- Output Short Circuit Protection
- Thermal Shutdown Protection
- 2-mm x 2-mm WSON Package

2 Applications

- Battery Powered IoT Devices
- Gaming Control
- Thermostat
- Portable Medical Equipment
- Supercap Backup System

3 Description

The TPS61021A provides a power supply solution for portable or smart devices powered by alkaline, NiMH, Li-Mn, or Li-ion batteries. The TPS61021A is capable of outputting 3.3-V voltage and 1.5-A current from a battery discharged to as low as 1.8 V. Capable of operating with 0.5-V input voltage enables the TPS61021A to extend the battery run time.

The TPS61021A operates at 2-MHz switching frequency at heavy load and enters power-save mode at light load to maintain high efficiency over the entire load current range. The device only consumes a 17-µA quiescent current from V_{OUT} in light load condition. During shutdown, the load is completely disconnected from the input. In addition, The TPS61021A provides 4.35-V output overvoltage protection, output short circuit protection, and thermal shutdown protection.

The TPS61021A offers a very small solution size due to low count of external components. It allows the use of small inductors and output capacitors with the 2-MHz switching frequency.

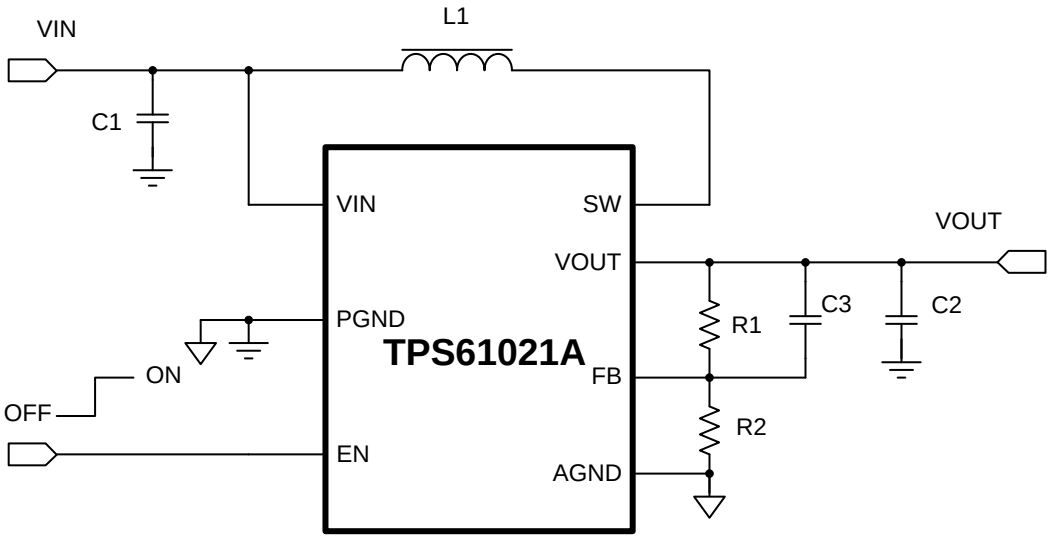
The TPS61021A is available in 2.0-mm x 2.0-mm WSON package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61021A	WSON (8)	2.00-mm x 2.00-mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



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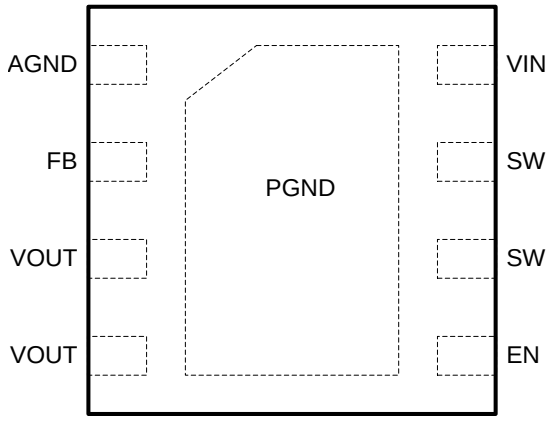
4 Revision History

DATE	REVISION	NOTES
June 2016	*	Initial release.

5 Pin Configuration and Functions

DSG Package
8-Pin WSON with Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	1	I	Signal ground of the IC
FB	2	I	Voltage feedback of adjustable output voltage
VOUT	3,4	PWR	Boost converter output
EN	5	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.
SW	6,7	PWR	The switch pin of the converter. It is connected to the drains of the internal power MOSFETs.
VIN	8	I	IC power supply input
PGND	9	PWR	Power ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage range at terminals(2)	EN, FB	DC	–0.3	3.6	V
	VIN, SW, VOUT	DC	–0.3	4.6	V
		10% duty cycle	–0.3	4.8	V
Operating junction temperature, T_J			–40	150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		0.5		4.4	V
V_{OUT}	Output voltage setting range		1.8		4.0	V
L	Effective inductance range		0.2	0.47	1.3	µH
C_{IN}	Effective input capacitance range		1.0	4.7		µF
C_{OUT}	Effective output capacitance range	$I_{OUT} \le 0.3$ A	3.0	10	200	µF
		$I_{OUT} > 0.3$ A	10	20	200	µF
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61021A DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

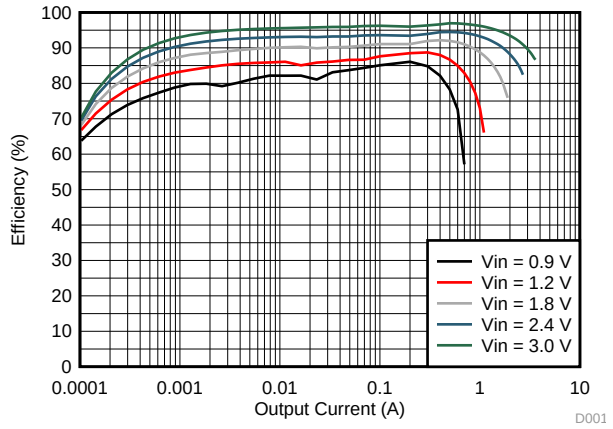
6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 2.4 V and V_{OUT} = 3.3 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		0.5		4.4	V
V_{IN_UVLO}	Under-voltage lockout threshold	V_{IN} rising		0.8	0.9	V
		V_{IN} falling	0.28	0.4	0.5	V
I_Q	Quiescent current into VIN pin	IC enabled, No load, No switching V_{IN} = 1.8 V to 3.6 V, V_{FB} = V_{REF} + 0.1 V, T_J up to 85°C			3.0	µA
	Quiescent current into VOUT pin	IC enabled, No load, No switching V_{OUT} = 1.8 V to 4.0 V, V_{FB} = V_{REF} + 0.1 V, T_J up to 85°C		17	30	µA
I_{SD}	Shutdown current into VIN and SW pin	IC disabled, V_{IN} = 1.8 V to 3.6 V, T_J up to 85°C		0.5	3.0	µA
OUTPUT						
V_{OUT}	Output voltage setting range		1.8		4.0	V
V_{REF}	Reference voltage at the FB pin	PWM mode	775	795	815	mV
		PFM mode		801		mV
V_{OVP}	Output over-voltage protection threshold	V_{OUT} rising	4.15	4.35	4.60	V
V_{OVP_HYS}	Over-voltage protection hysteresis			0.1		V
I_{FB_LKG}	Leakage current at FB pin				20	nA
I_{SW_LKG}	Leakage current into SW pin	IC disabled, T_J up to 85°C			3.0	µA
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{OUT} = 4.0 V, T_J up to 85°C		1	2	µA
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on resistance	V_{OUT} = 3.3 V		51		mΩ
	Low-side MOSFET on resistance	V_{OUT} = 3.3 V		58		mΩ
f_{SW}	Switching frequency	V_{IN} = 2.4 V, V_{OUT} = 3.3 V, PWM mode		2.0		MHZ
t_{OFF_min}	Minimum off time			80	120	ns
I_{LIM_SW}	Valley current limit	V_{IN} = 2.4 V, V_{OUT} = 3.3 V	3.0	4.3		A
LOGIC INTERFACE						
V_{EN_H}	EN Logic high threshold	V_{IN} > 1.2 V			0.84	V
		V_{IN} ≤ 1.2 V			0.7 x V_{IN}	
V_{EN_L}	EN Logic Low threshold	V_{IN} > 1.2 V	0.36			V
		V_{IN} ≤ 1.2 V	0.3 x VIN			
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

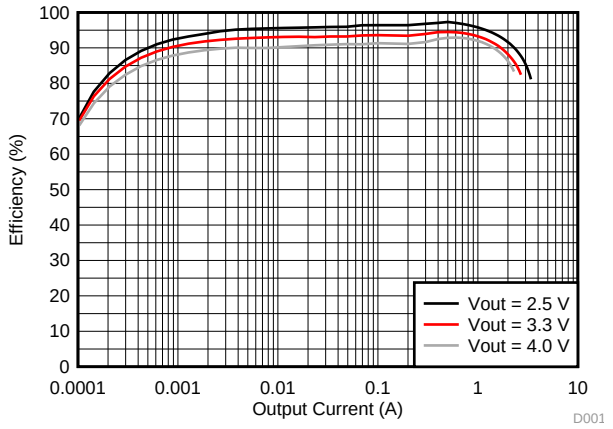
6.6 Typical Characteristics

V_{IN} = 2.4 V, V_{OUT} = 3.3 V, T_J = 25°C, unless otherwise noted



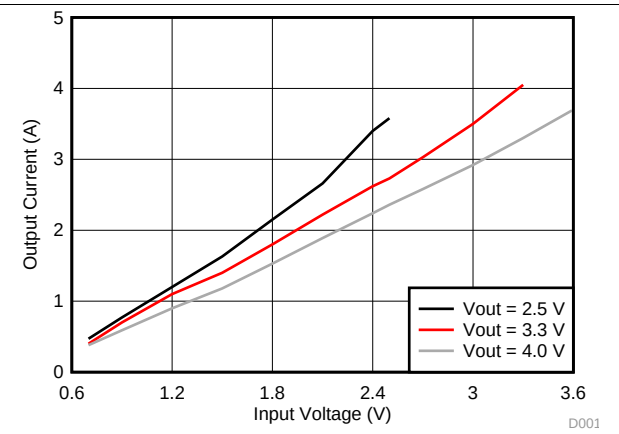
V_{IN} = 0.9 V, 1.2 V, 1.8 V, 2.4 V, 3.0 V, and V_{OUT} = 3.3 V

Figure 1. Load Efficiency with Different Input



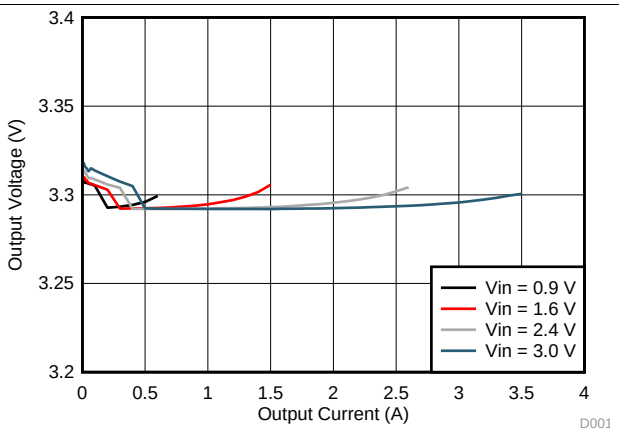
V_{IN} = 2.4 V, and V_{OUT} = 2.5 V, 3.3 V, 4.0 V

Figure 2. Load Efficiency with Different Output



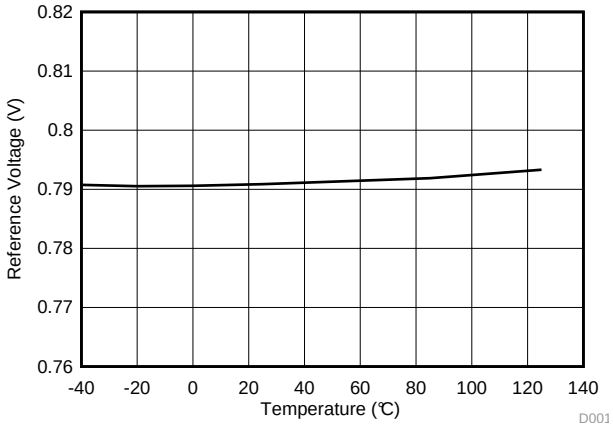
V_{IN} = 0.7 V to 3.6 V, V_{OUT} = 2.5 V, 3.3 V, 4.0 V

Figure 3. Maximum Output Current vs Input Voltage



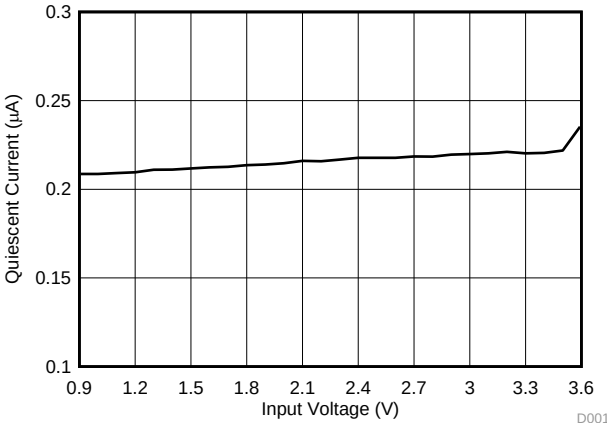
V_{IN} = 0.9 V, 1.6 V, 2.4 V, 3.0 V, and V_{OUT} = 3.3 V

Figure 4. Load Regulation



V_{IN} = 2.4 V, V_{OUT} = 3.3 V, T = –40°C to 125°C

Figure 5. Reference Voltage vs Temperature

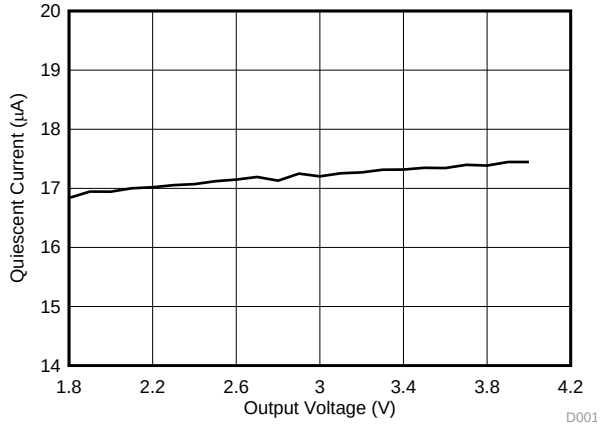


V_{IN} = 0.9 V to 3.6 V, V_{OUT} = 4.0 V, No switching

Figure 6. Quiescent Current into VIN vs Input Voltage

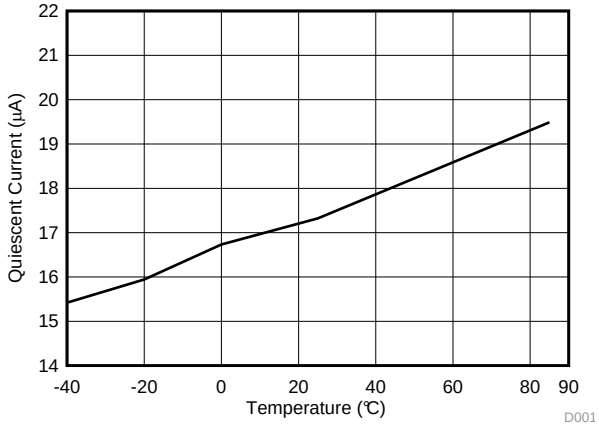
Typical Characteristics (continued)

V_{IN} = 2.4 V, V_{OUT} = 3.3 V, T_J = 25°C, unless otherwise noted



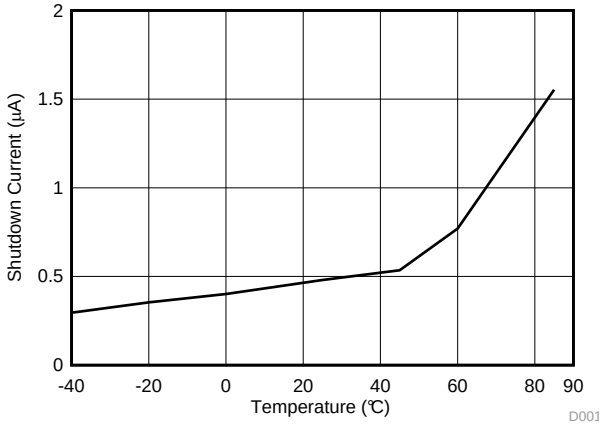
V_{IN} = 1.2 V, V_{OUT} = 1.8 V to 4.0 V, No switching

Figure 7. Quiescent Current into VOUT vs Output Voltage



V_{IN} = 2.4 V, V_{OUT} = 3.3 V, No switching, T = –40°C to 85°C

Figure 8. Quiescent Current into VOUT vs Temperature



V_{IN} = 2.4 V, Into VIN and SW, T = –40°C to 85°C

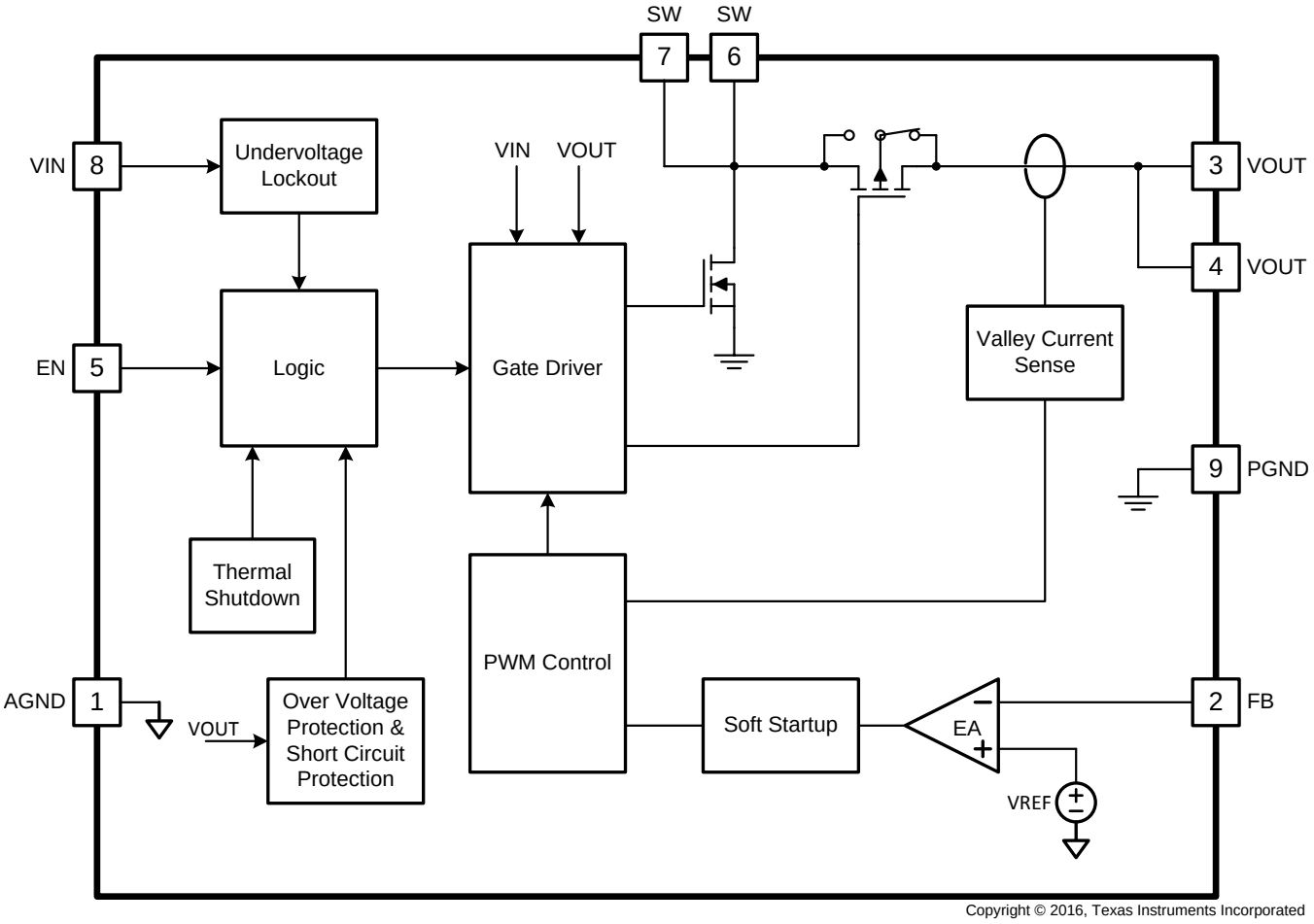
Figure 9. Shutdown Current vs Temperature

7 Detailed Description

7.1 Overview

The TPS61021A synchronous step-up converter is designed to operate from an input voltage supply range between 0.5 V and 4.4 V with 3-A valley switch current limit. The TPS61021A typically operates at a quasi-constant frequency pulse width modulation (PWM) at moderate to heavy load currents. The switching frequency is 2 MHz when the input voltage is above 1.5 V. The switching frequency reduces down to 1 MHz when the input voltage goes down from 1.5 V to 1 V. At light load currents, the TPS61021A converter operates in power-save mode with pulse frequency modulation (PFM). During PWM operation, the converter uses adaptive constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small inductor and ceramic capacitors. Internal loop compensation simplifies the design process while minimizing the number of external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Under-Voltage Lockout

The TPS61021A has a built-in under-voltage lockout (UVLO) circuit to ensure the device working properly. When the input voltage is above the UVLO rising threshold of 0.9 V, the TPS61021A can be enabled to boost the output voltage. After the TPS61021A starts up and the output voltage is above 1.6 V, the TPS61021A can work with the input voltage as low as 0.5 V.

Feature Description (continued)

7.3.2 Enable and Soft Start

When the input voltage is above the under-voltage lockout (UVLO) rising threshold and the EN pin is pulled to logic high voltage, the TPS61021A is enabled and starts up. At the beginning, the switching frequency and current limit are internally controlled. The load capability is limited. After the output voltage is above 1.6 V, the peak current limit is determined by the output of an internal error amplifier which compares the feedback of the output voltage and the internal reference voltage. Because the output voltage is below the setting target, the peak current limit rises and thus the output voltage ramps quickly. The soft startup time varies with the different output capacitance and load condition. The typical startup time is around 200 μs for a 44-μF output capacitor with no load.

7.3.3 Switching Frequency

The TPS61021A switches at a quasi-constant 2-MHz frequency when the input voltage is above 1.5 V. When the input voltage declines from 1.5 V to 1 V, the switching frequency will be reduced gradually to 1-MHz to improve the efficiency and get higher boost ratio. When the input voltage is below 1 V, the switching frequency is fixed at a quasi-constant 1 MHz.

7.3.4 Current Limit Operation

The TPS61021A employs a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier switch.

When the load current is increased such that the inductor current is above the current limit within the whole switching cycle time, the off-time is increased to allow the inductor current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached, the output voltage decreases during further load increase.

The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1-D) \times \left(I_{LIM} + \frac{1}{2} \Delta I_{L(P-P)} \right) \quad (1)$$

Where:

D is the duty cycle

$\Delta I_{L(P-P)}$ is the inductor ripple current

The duty cycle can be estimated by Equation 2.

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (2)$$

Where:

V_{OUT} is the output voltage of the boost converter

V_{IN} is the input voltage of the boost converter

η is the efficiency of the converter, use 90% for most applications

And the peak-to-peak inductor ripple current is calculated by Equation 3.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (3)$$

Where:

L is the inductance value of the inductor

f_{SW} is the switching frequency

D is the duty cycle

V_{IN} is the input voltage of the boost converter

Feature Description (continued)

7.3.5 Pass-Through Operation

When the input voltage is higher than the setting output voltage, the output voltage is higher than the target regulation voltage. When the output voltage is 101% of the setting target voltage, the TPS61021A stops switching and turns on the high side PMOS FET. The device works in pass-through mode. The output voltage is the input voltage minus the voltage drop across the dc resistance (DCR) of the inductor and the on-resistance ($R_{DS(on)}$) of the PMOS FET. When the output voltage drops below the 98% of the setting target voltage as the input voltage declines or the load current increases, the TPS61021A resumes switching again to regulate the output voltage.

7.3.6 Over-Voltage Protection

The TPS61021A has an output over-voltage protection (OVP) to protect the device in case that the external feedback resistor divider is wrongly populated. When the output voltage is above 4.35 V typically, the device stops switching. Once the output voltage falls 0.1 V below the OVP threshold, the device resumes operating again. To prevent the high overshoot voltage during OVP when the FB pin voltage is too much lower than the internal reference voltage, the TPS61021A limits the valley swtich current to approximate 100 mA when the FB pin voltage is below 0.2 V and the output voltage is above 2.9V.

7.3.7 Output Short-to-Ground Protection

The TPS61021A starts to limit the output current when the output voltage is below 1.6 V. The lower the output voltage reaches, the smaller the output current is. When the output voltage is below 1 V, the output current is limited to approximate 100 mA. Once the short circuit is released, the TPS61021A goes through the soft startup again to output the regulated voltage.

7.3.8 Thermal Shutdown

The TPS61021A goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown temperature threshold less the hysteresis, typically 130°C, the device starts operating again.

7.4 Device Functional Modes

The TPS61021A has two switching operation modes, PWM mode in moderate to heavy load conditions and power save mode with pulse frequency modulation (PFM) in light load conditions.

7.4.1 PWM Mode

The TPS61021A uses a quasi-constant 2.0-MHz frequency pulse width modulation (PWM) at moderate to heavy load current. Based on the input voltage to output voltage ratio, a circuit predicts the required on-time. At the beginning of the switching cycle, the NMOS switching FET, shown in the functional block diagram, is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the on-time expires, the main switch NMOS FET is turned off, and the rectifier PMOS FET is turned on. The inductor transfers its stored energy to replenish the output capacitor and supply the load. The inductor current declines because the output voltage is higher than the input voltage. When the inductor current hits a value which the error amplifier outputs, the next switching cycle starts again.

The TPS61021A has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value and output capacitor value for stable operation.

Device Functional Modes (continued)

7.4.2 Power Save Mode

The TPS61021A integrates a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. When the load current decreases, the inductor valley current set by the output of the error amplifier declines to regulate the output voltage. When the inductor valley current hits the low limit of approximate 100 mA, the output voltage will exceed the setting voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TPS61021A goes into the power save mode. In the power save mode, when the FB voltage rises and hits the PFM reference voltage, the device continuous switching for several cycles because of the delay time of the internal comparator. Then it stops switching. The load is supplied by the output capacitor and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

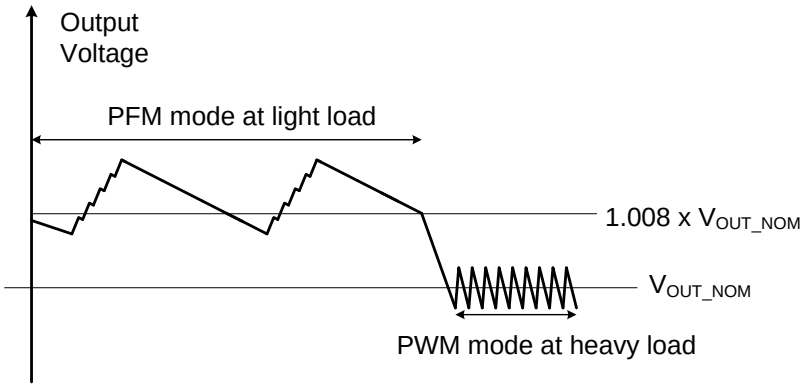


Figure 10. Output Voltage in PWM Mode and PFM Mode

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61021A is a synchronous boost converter designed to operate from an input voltage supply range between 0.5 V and 4.4 V with 3-A valley switch current limit. The TPS61021A typically operates at a quasi-constant 2-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents when the input voltage is above 1.5 V. The switching frequency changes to 1-MHz gradually with the input voltage changing from 1.5 V to 1 V to get better efficiency and high step-up ratio. At light load currents, the TPS61021A converter operates in power-save mode with pulse frequency modulation (PFM) to achieve high efficiency over the entire load current range.

8.2 Typical Application

The TPS61021A provides a power supply solution for portable or smart devices powered by batteries or super-capacitors. With 3-A switch current capability, the TPS61021A can output 3.3 V and 1.5 A from two alkaline batteries in series even if the battery voltage is down to 1.8 V.

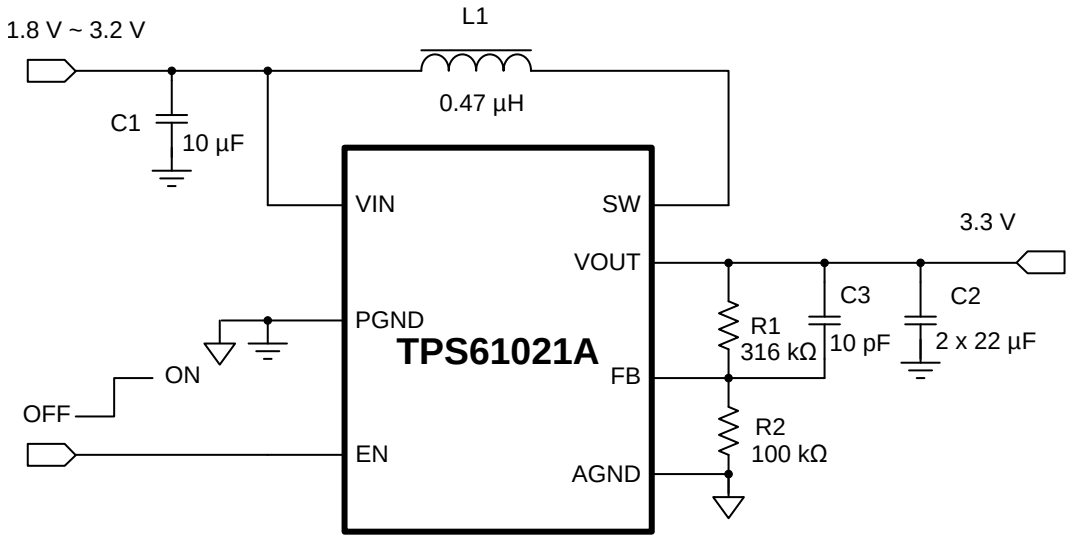


Figure 11. 2-Cell Alkaline Battery to 3.3-V Boost Converter

8.2.1 Design Requirements

The design parameters are listed in Table 1.

Table 1. Design Parameters

PARAMETERS	VALUES
Input voltage	1.8 V to 3.2 V
Output voltage	3.3 V
Output current	1.5 A
Output voltage ripple	±50 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in Figure 11). When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus the resistor divider is determined by Equation 4.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (4)$$

Where:

V_{OUT} is the regulated output voltage

V_{REF} is the internal reference voltage at the FB pin

For best accuracy, R2 should be kept smaller than 400 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving highest efficiency at low load currents.

8.2.2.2 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TPS61021A is designed to work with inductor values between 0.33 µH and 1.0 µH. Follow Equation 5 to Equation 7 to calculate the inductor's peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margins, choose the inductor value with -30% tolerances, and low power-conversion efficiency for the calculation.

In a boost regulator, the inductor dc current can be calculated by Equation 5.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (5)$$

Where:

V_{OUT} is the output voltage of the boost converter

I_{OUT} is the output current of the boost converter

V_{IN} is the input voltage of the boost converter

η is the power conversion efficiency, use 90% for most applications

The inductor ripple current is calculated by Equation 6.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (6)$$

Where:

D is the duty cycle, which can be calculated by Equation 2

L is the inductance value of the inductor

f_{SW} is the switching frequency

V_{IN} is the input voltage of the boost converter

Therefore, the inductor peak current is calculated by Equation 7.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (7)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. The inductor's saturation current must be higher than the calculated peak inductor current. Table 2 lists the recommended inductors for the TPS61021A.

Table 2. Recommended Inductors for the TPS61021A

PART NUMBER	L(µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (LxWxH)	VENDOR(1)
XFL4015-471ME	0.47	8.36	6.6	4.0×4.0×1.5	Coilcraft
744383360047	0.47	22	8.0	3.0x3.0x2.0	Wurth Elecktronik
DFE252012P-R47M	0.47	27	5.7	2.5×2.0×1.2	Toko
XFL4020-102ME	1.0	11.9	5.4	4.0×4.0×2.1	Coilcraft

(1) See Third-party Products disclaimer

8.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple voltage can be calculated by Equation 8.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (8)$$

Where:

D_{MAX} is the maximum switching duty cycle
V_{RIPPLE} is the peak to peak output ripple voltage
I_{OUT} is the maximum output current
f_{SW} is the switching frequency

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. The output peak to peak ripple voltage caused by the ESR of the output capacitors can be calculated by Equation 9.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (9)$$

Care must be taken when evaluating a ceramic capacitor's derating under dc bias voltage, aging, and ac signal. For example, the dc bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

It is recommended to use the X5R or X7R ceramic output capacitor in the range of 10 µF to 200 µF effective capacitance. For output current less than 300 mA, the effective output capacitance could be reduced to 3.0 µF. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

8.2.2.4 Feedforward Capacitor Selection

A feedforward capacitor between the VOUT pin and FB pin induces a pair of zero and pole in the loop transfer function. Setting the proper zero frequency can increase the phase margin to improve the loop stability. The TPS61021A needs a feedforward capacitor (C3 in Figure 11) in most applications. It is recommended to set the zero frequency (f_{FFZ}) to 50 kHz when the effective output capacitance is less than 40 µF. For large output capacitance more than 40 µF, it is recommended to set the zero frequency (f_{FFZ}) to 5 kHz. The value of the feedforward capacitor can be calculated by Equation 10.

$$C3 = \frac{1}{2\pi \times f_{FFZ} \times R1} \quad (10)$$

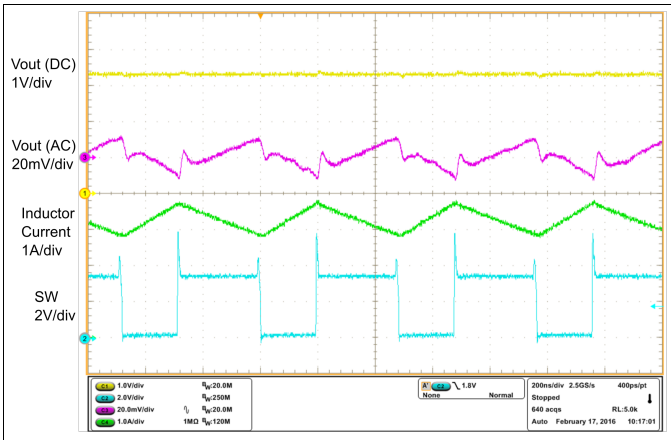
Where:

R1 is the resistor between the VOUT pin and FB pin
f_{FFZ} is the zero frequency created by the feedforward capacitor

8.2.2.5 Input Capacitor Selection

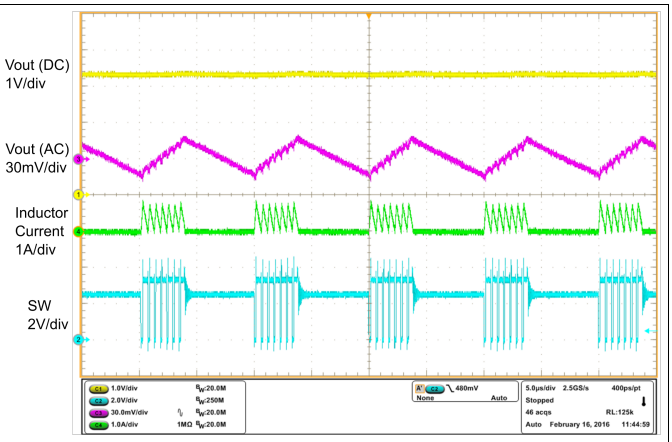
Multilayer X5R or X7R ceramic capacitors are excellent choices for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 10-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional bulk capacitance (tantalum or aluminum electrolytic capacitor) should in this circumstance be placed between ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

8.2.3 Application Curves



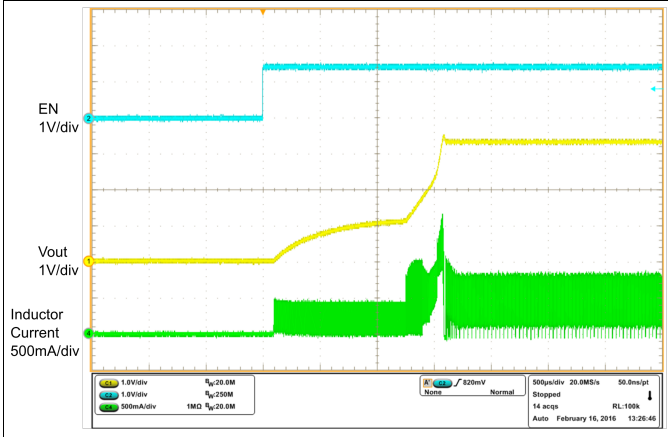
V_{IN} = 2.4 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A

Figure 12. Switching Waveform at Heavy Load



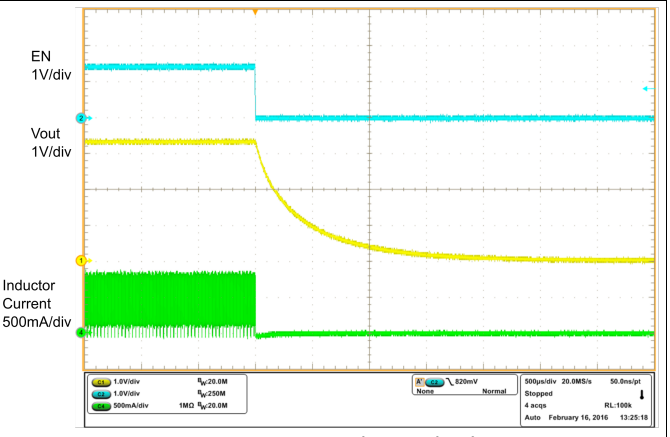
V_{IN} = 2.4 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA

Figure 13. Switching Waveform at Light Load



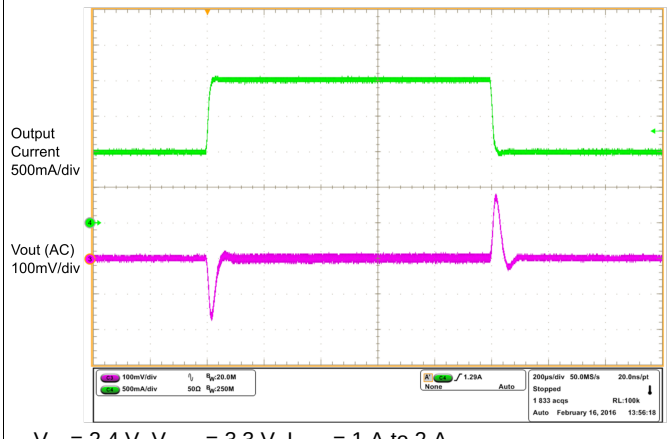
V_{IN} = 2.4 V, V_{OUT} = 3.3 V, 12 Ω resistance load

Figure 14. Startup Waveform



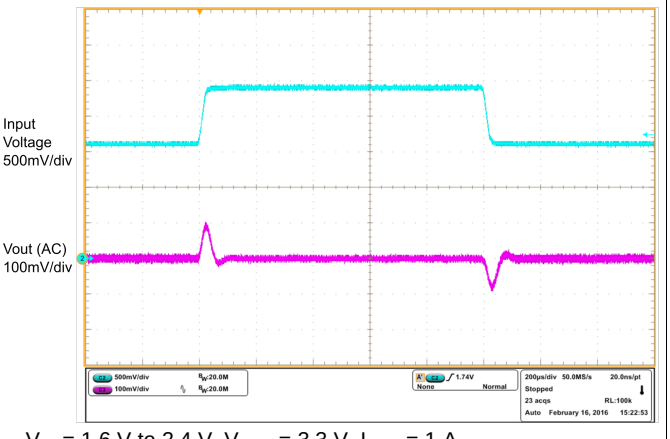
V_{IN} = 2.4 V, V_{OUT} = 3.3 V, 12 Ω resistance load

Figure 15. Shutdown Waveform



V_{IN} = 2.4 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A to 2 A

Figure 16. Load Transient



V_{IN} = 1.6 V to 2.4 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A

Figure 17. Line Transient

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.5 V to 4.4 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100 µF. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS61021A.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs not only to be close to the VIN pin, but also to the PGND pin in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the PGND pin to reduce the overshoot at the SW pin and VOUT pin.

10.2 Layout Example

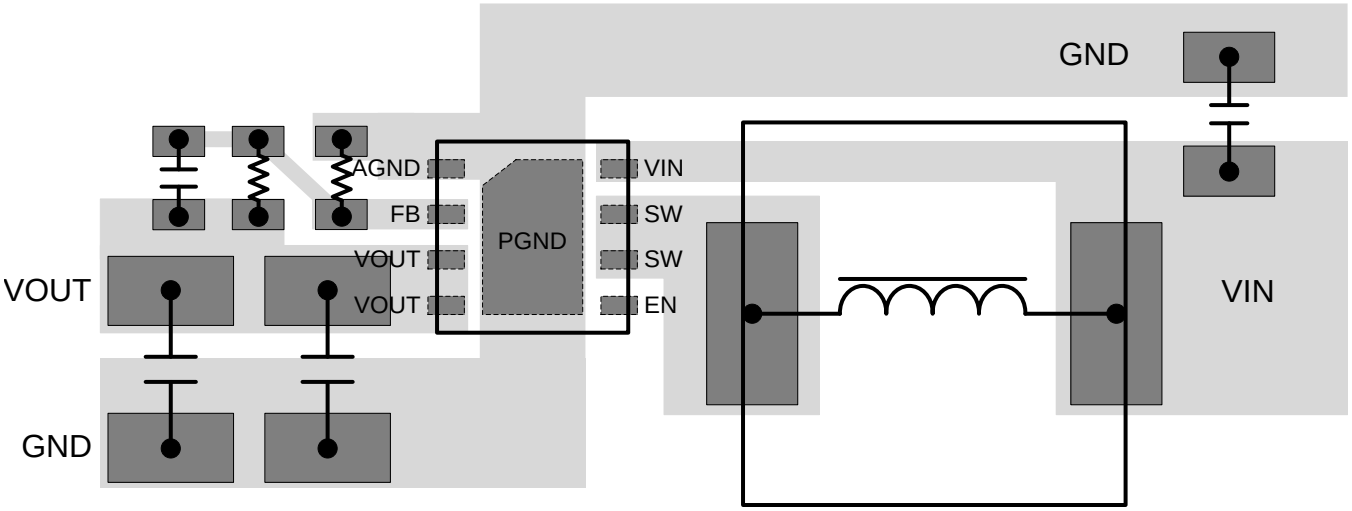


Figure 18. Layout Example

10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 11.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{11}$$

Where:

T_A is the maximum ambient temperature for the application

$R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The TPS61021A comes in a thermally-enhanced WSON package. This package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper and soldering the thermal pad to a large ground plate to enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
TPS61021ADSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	–40 to 125	11G
TPS61021ADSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	–40 to 125	11G

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

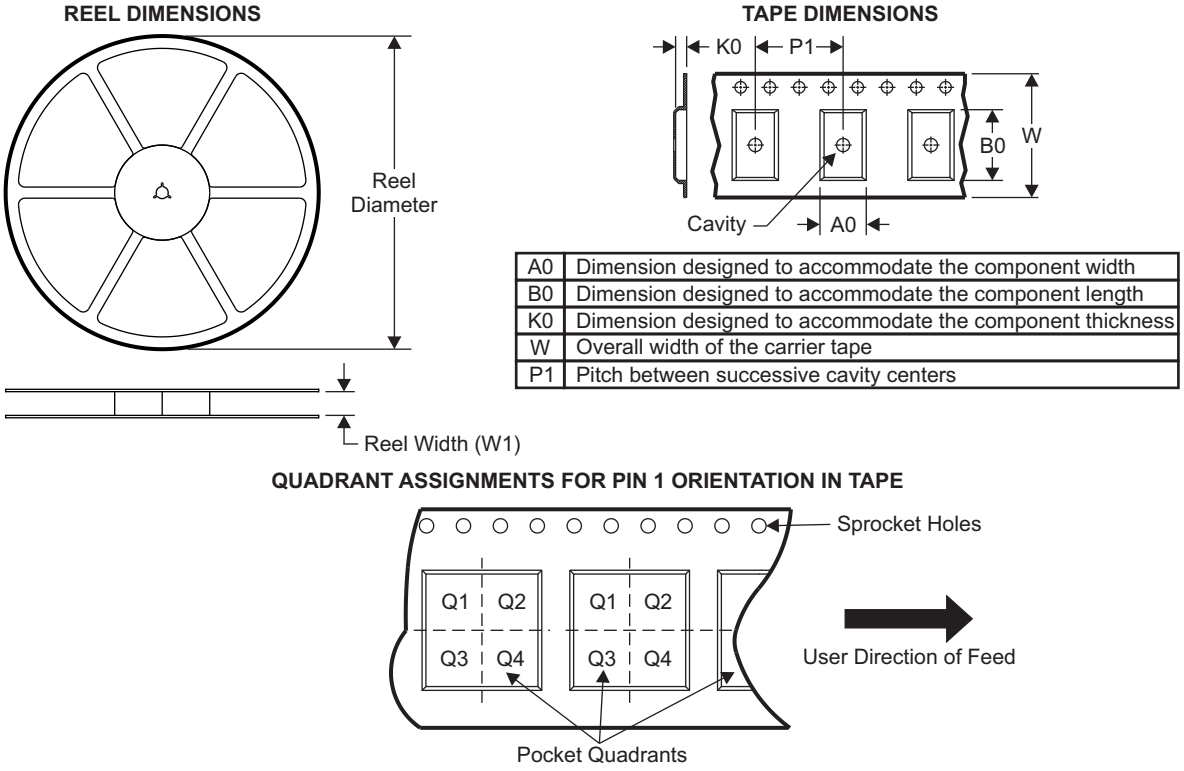
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

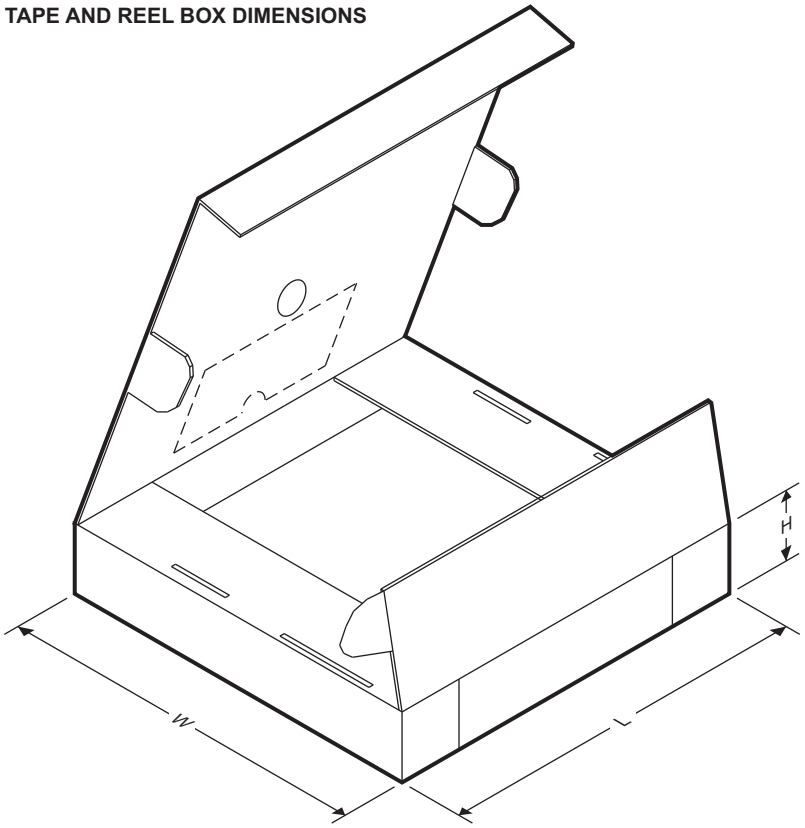
12.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

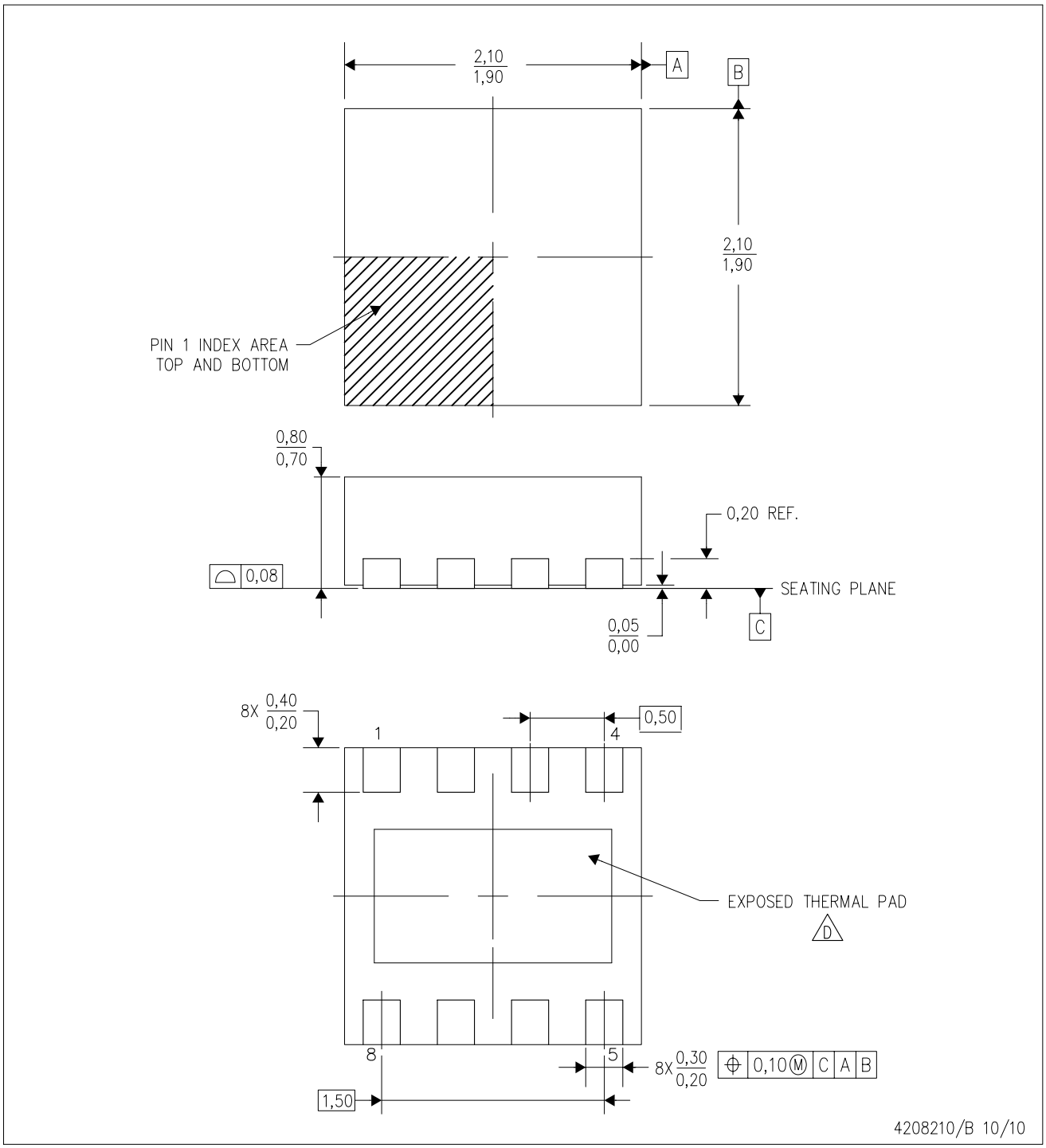
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61021ADSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61021ADSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61021ADSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS61021ADSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

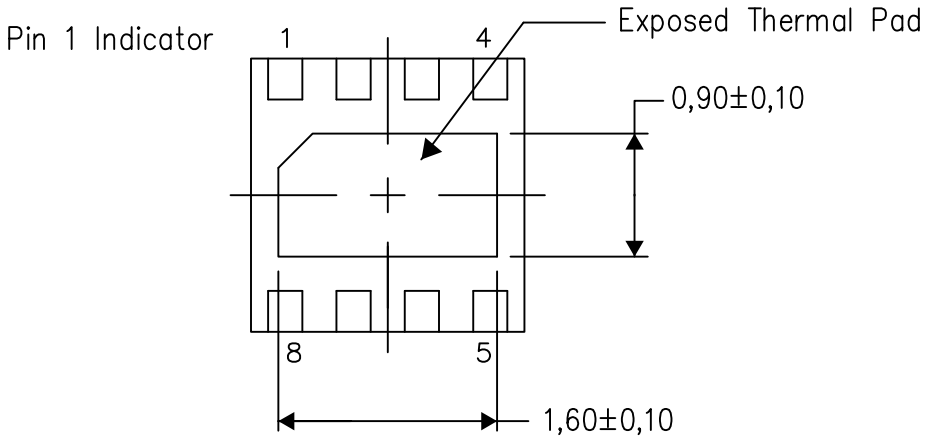
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



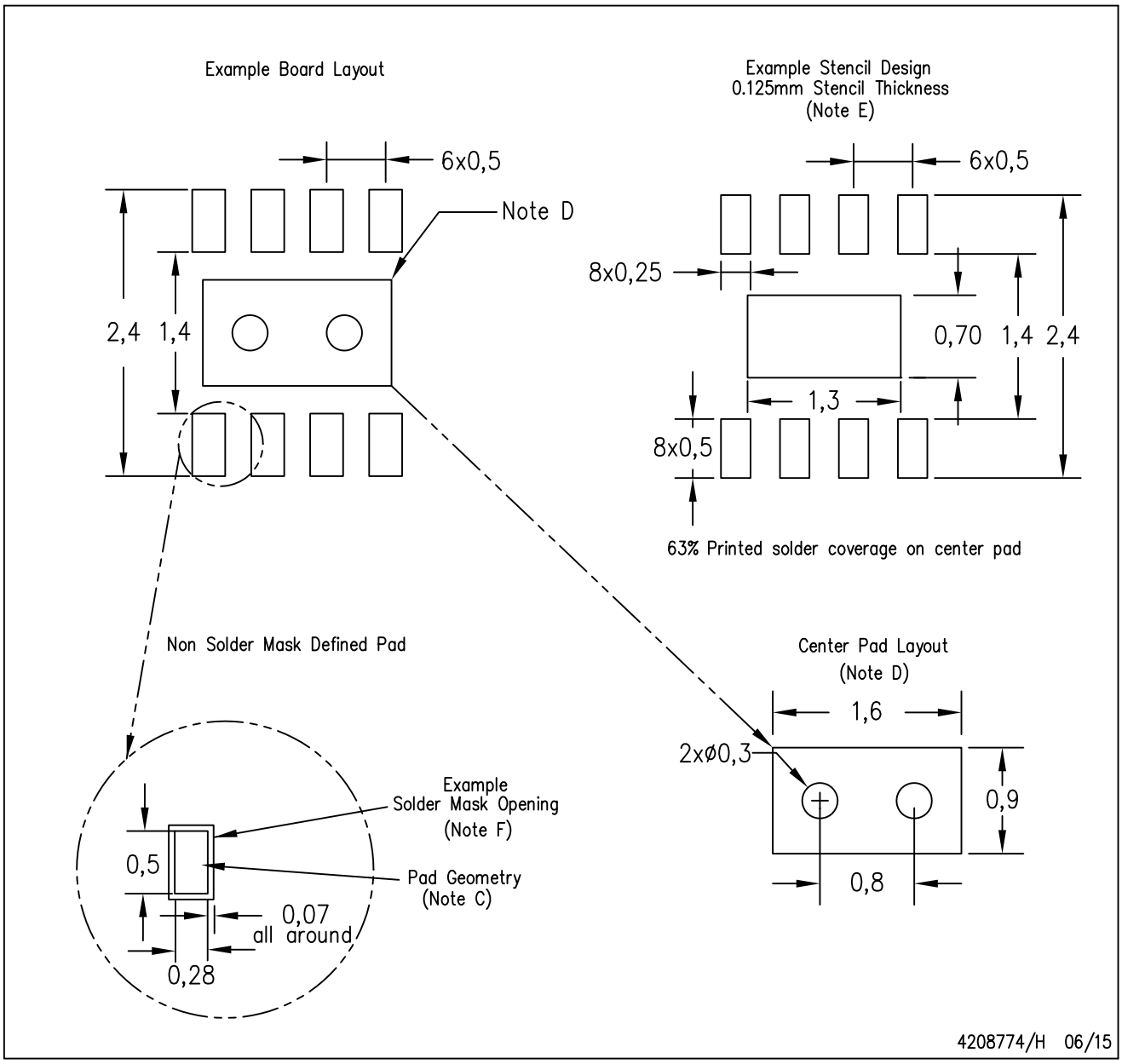
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61021ADSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11G	Samples
TPS61021ADSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11G	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

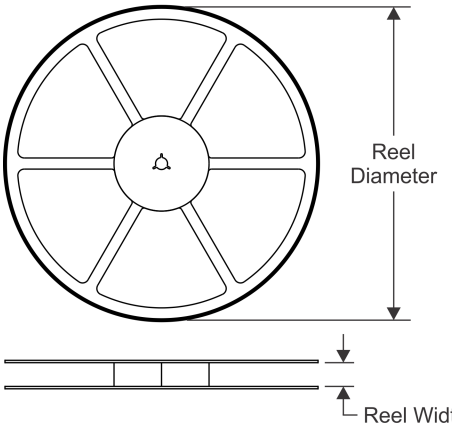
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

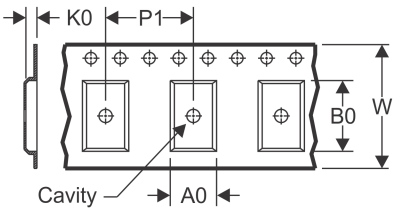
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

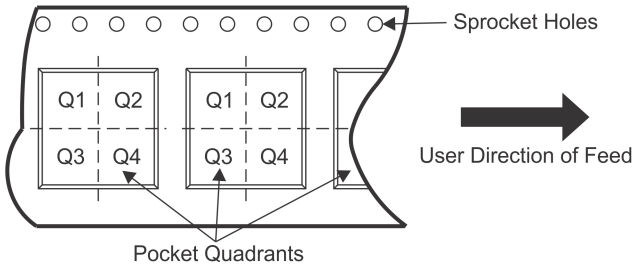


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

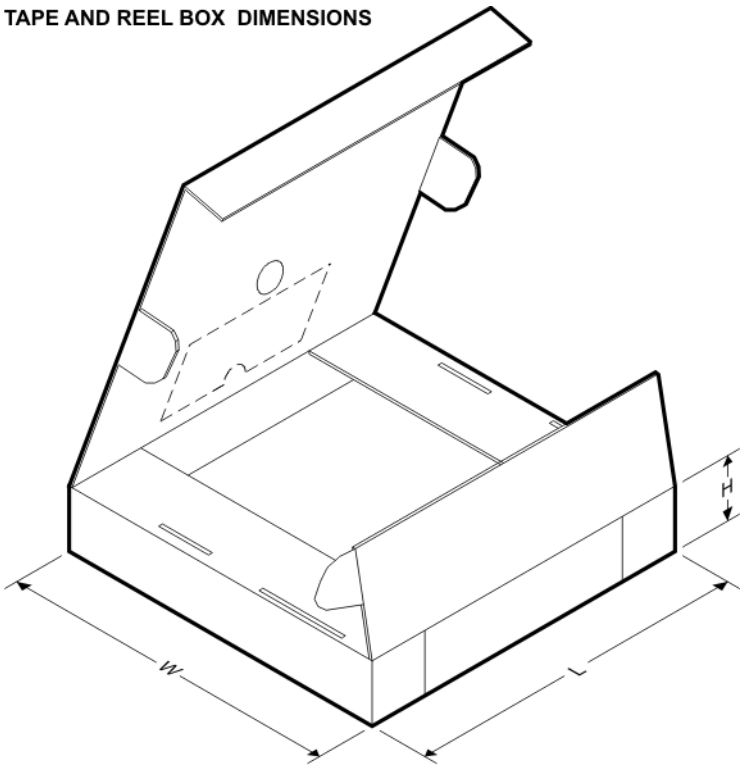
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61021ADSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61021ADSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
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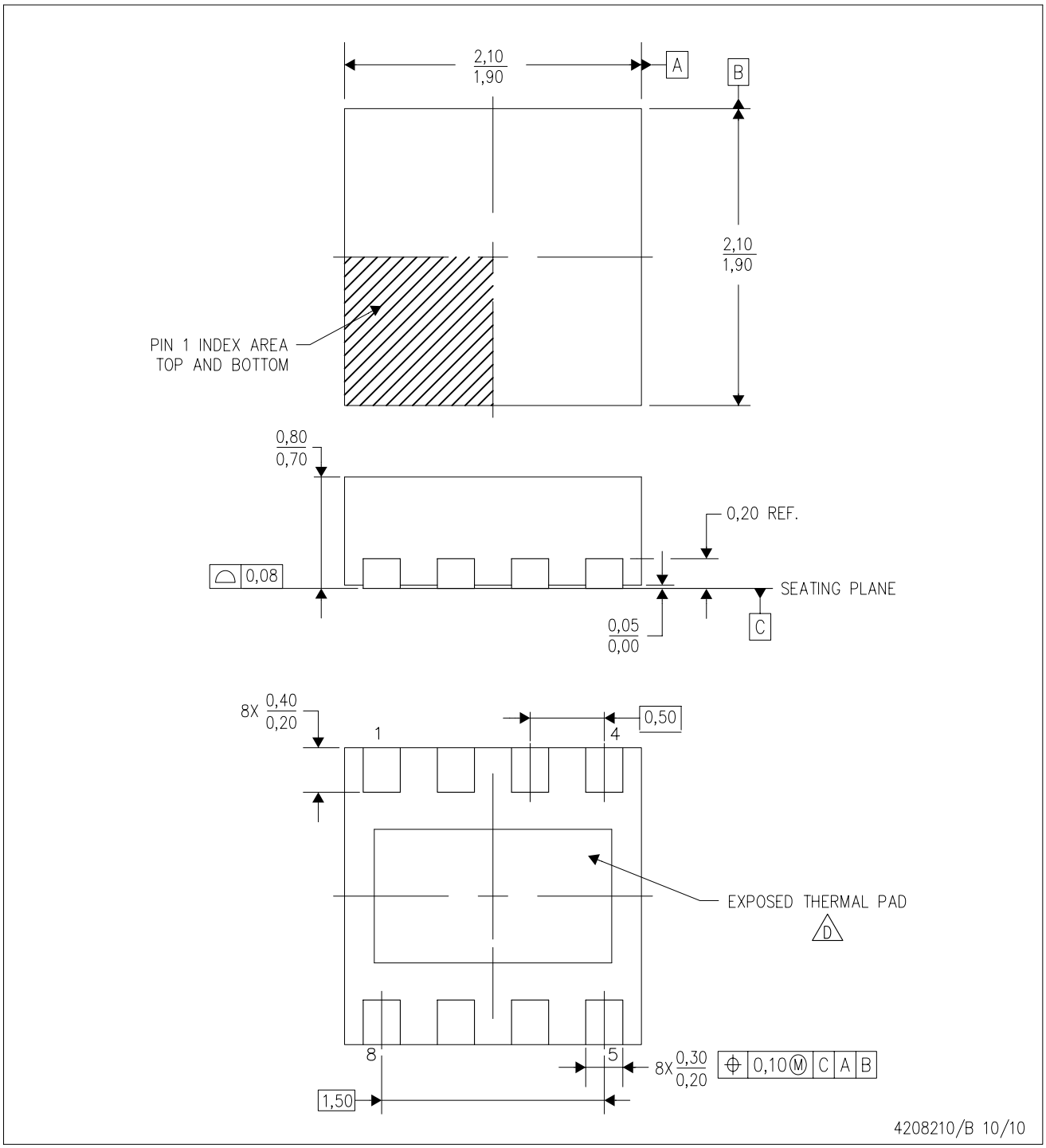
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

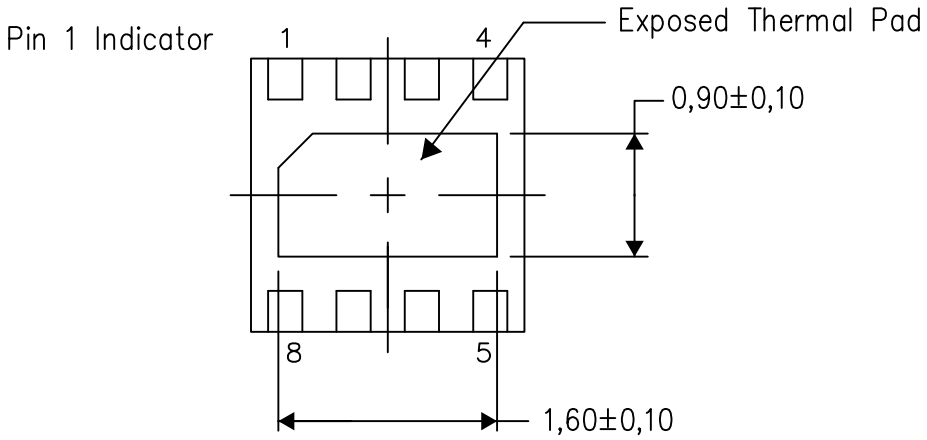
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



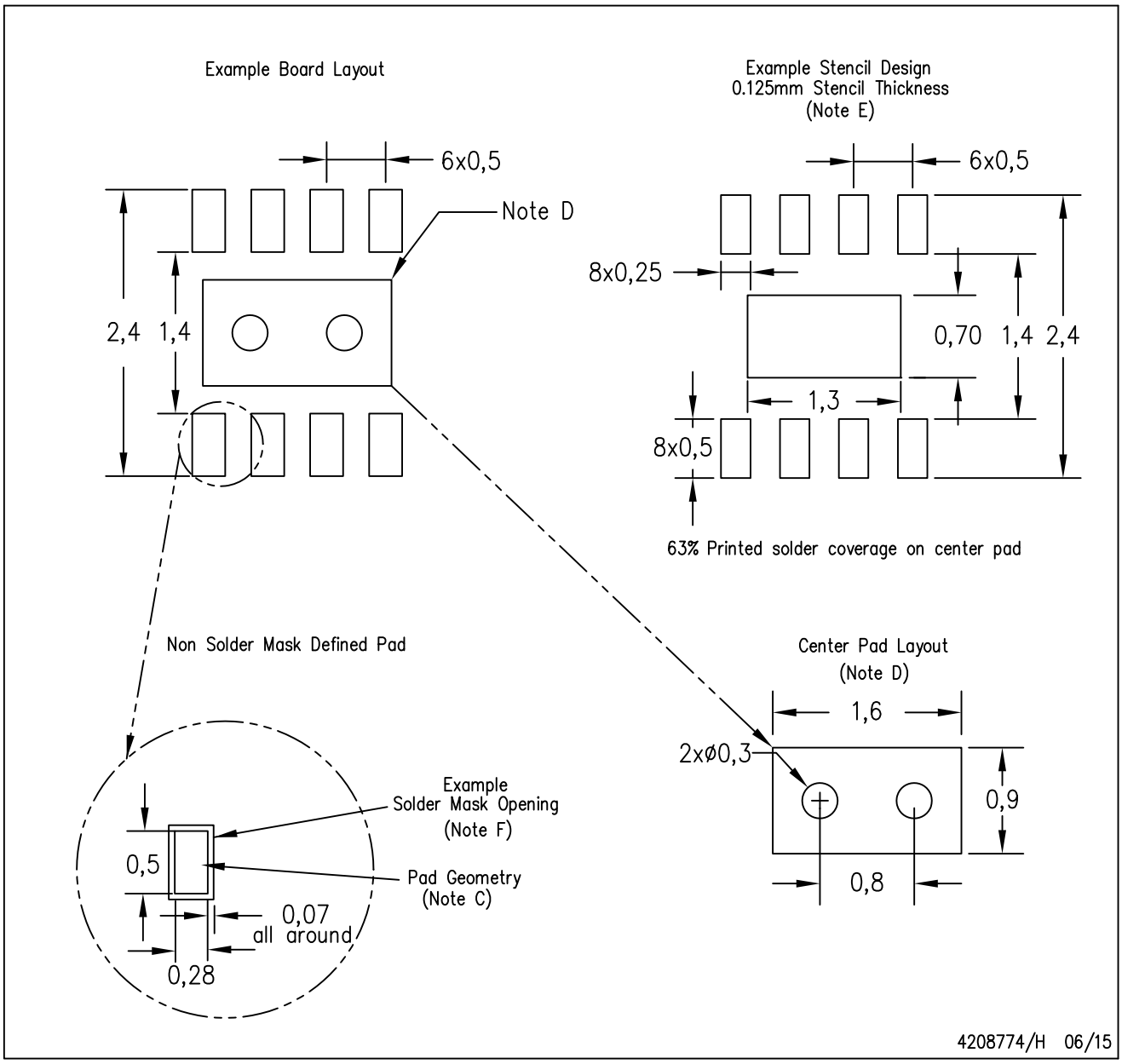
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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