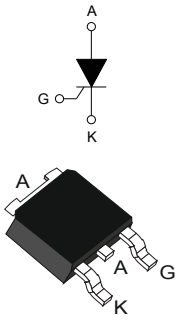
TN1605H-8B

Datasheet

16 A 800 V high temperature SCR thyristor in DPAK package



DPAK

Features

- High junction temperature: $T_j$max. = 150 °C
- V_{DRM} / V_{RRM} = 800 V
- V_{DSM} / V_{RSM} = 900 V
- Tight I_{GT} spread: 2 to 6 mA
- High static immunity dV/dt = 500 V/µs at 150 °C
- High turn-on rise dI/dt at 100 A/µs
- Halogen-free molding, lead-free plating
- ECOPACK2 compliant

Applications

- Inrush current limiting circuits in AC/DC converters
- General purpose AC line load switching
- Heating resistor control, solid state relays
- Crowbar and power bus discharge circuits

Product status
TN1605H-8B

Product summary	
Order code	TN1605H-8B
Package	DPAK
$I_{T(RMS)}$	16 A
V_{DRM}/V_{RRM}	800 V
T_j max.	150 °C

Description

Thanks to its operating junction temperature up to 150°C, the TN1605H-8B offers high thermal performance operation up to 16 A rms in a DPAK package.

Its trade-off noise immunity (dV/dt = 500 V/µs) versus its gate triggering current (maximum I_{GT} = 6 mA) and its turn-on current rise (dI/dt = 100 A/µs) allows to design robust and compact control circuit for voltage regulator in motorbikes and industrial drives, overvoltage crowbar protection, motor control circuits in power tools and kitchen appliances and inrush current limiting circuits.

1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)		T_C = 134 °C	16	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)		T_C = 134 °C	10	A
			T_C = 138 °C	8	
			T_C = 142 °C	6	
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25 °C)		t_P = 8.3 ms	153	A
			t_P = 10 ms	140	
I^2t	I^2t value for fusing		t_P = 10 ms	98	A²s
V_{DRM}, V_{RRM}	Repetitive peak off-state voltage			800	V
V_{DSM}, V_{RSM}	Non repetitive peak off-state voltage		t_P = 10 ms	900	V
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT}, t_r < 100 ns		f = 60 Hz	100	A/µs
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 150 °C	4	A
$P_{G(AV)}$	Average peak gate power dissipation		T_j = 150 °C	1	W
V_{RGM}	Maximum peak reverse gate voltage			5	V
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +150	

Table 2. Electrical characteristics (T_j = 25 °C unless otherwise specified)

Symbol	Test conditions				Value	Unit
I_{GT}	V_D = 12 V, R_L = 30 Ω			Min.	2	mA
				Max.	6	
V_{GT}					1.3	V
V_{GD}	V_D = 600 V, R_L = 3.3 kΩ		T_j = 150 °C	Min.	0.15	V
I_H	I_T = 500 mA, gate open			Max.	20	mA
I_L	I_G = 1.2 x I_{GT} max.			Max.	40	mA
dV/dt	V_{OUT} = 536 V, gate open		T_j = 150 °C	Min.	500	V/µs
t_{gt}	I_T = 32 A, V_D = 536 V, I_G = 12 mA, (dI_G/dt) max = 0.2 A/µs			Typ.	1.9	µs
t_q	I_T = 32 A, V_D = 536 V, V_R = 25 V, dV_D/dt = 20 V/µs		T_j = 150 °C	Typ.	25	µs

Table 3. Static characteristics

Symbol	Test conditions			Value	Unit
V_{TM}	I_{TM} = 32 A, t_p = 380 µs	T_j = 25 °C	Max.	1.55	V
V_{TO}	Threshold voltage	T_j = 150 °C	Max.	0.9	
R_D	Dynamic resistance	T_j = 150 °C	Max.	22	mΩ
I_{DRM}, I_{RRM}	V_D = V_{DRM}, V_R = V_{RRM}	T_j = 25 °C	Max.	1	µA
		T_j = 150 °C		4.5	mA
	V_D = 400 V, V_R = 400 V	T_j = 150 °C		1.5	mA

Table 4. Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Max.	1.1	°C/W
$R_{th(j-a)}$	Junction to ambient, S(1) = 1.5 cm²	Typ.	70	

1. *S : Copper surface under DPAK tab, copper thickness 70 µm*

1.1 Characteristics curves

Figure 1. Maximum average power dissipation versus average on-state current

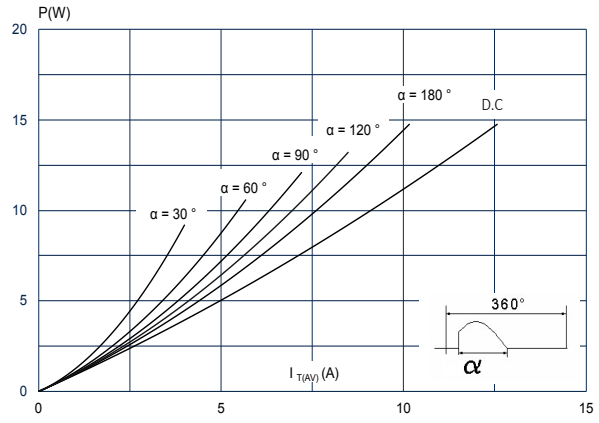


Figure 2. Average and DC on-state current versus case temperature

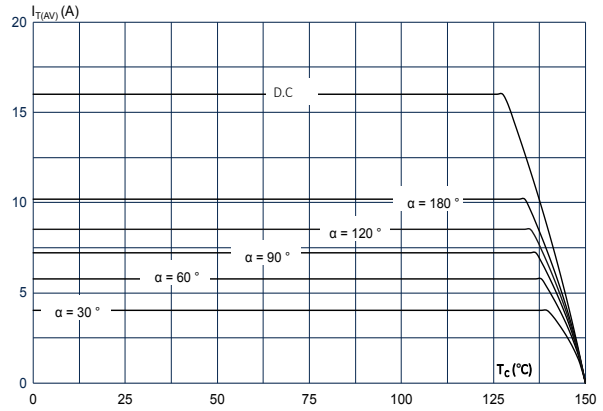


Figure 3. Average and D.C. on-state current versus ambient temperature

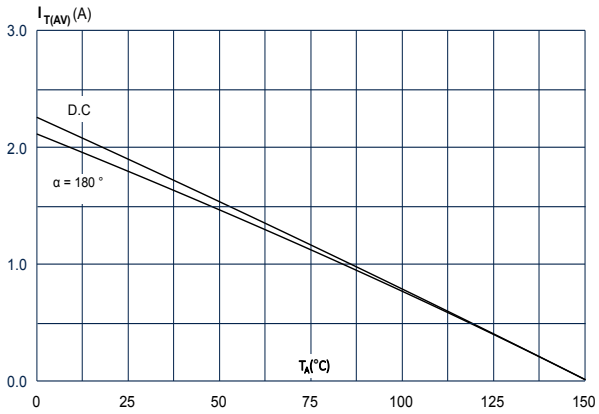


Figure 4. On-state characteristics (maximum values)

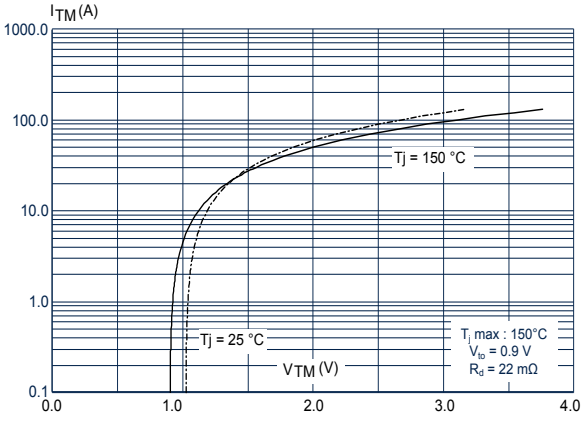


Figure 5. Relative variation of thermal impedance junction to case and junction to ambient versus pulse duration

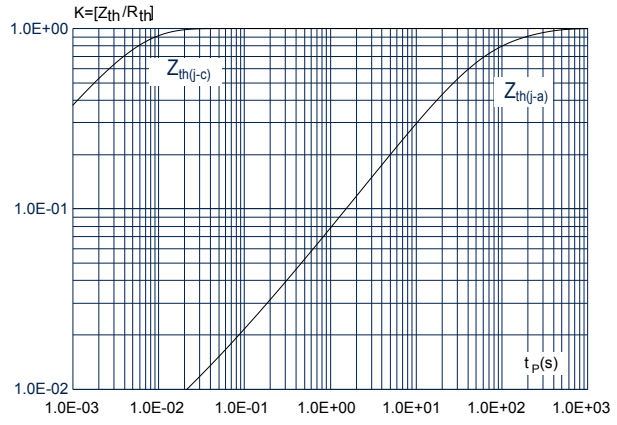


Figure 6. Surge peak on-state current versus number of cycles

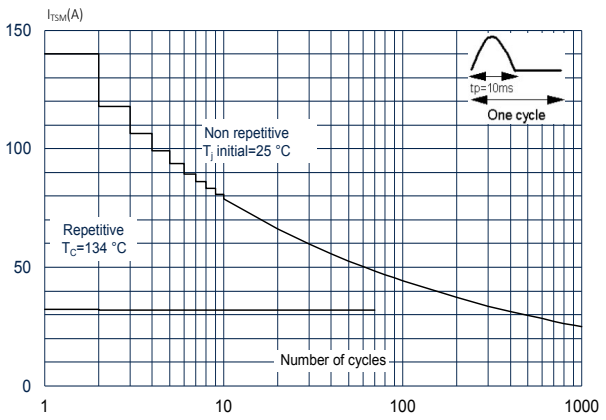


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms

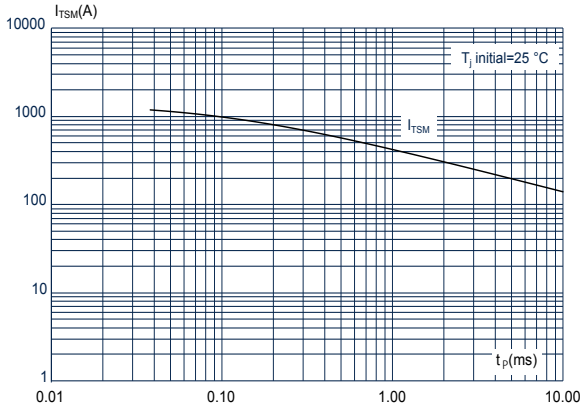


Figure 8. Relative variation of holding current and latching current versus junction temperature (typical values)

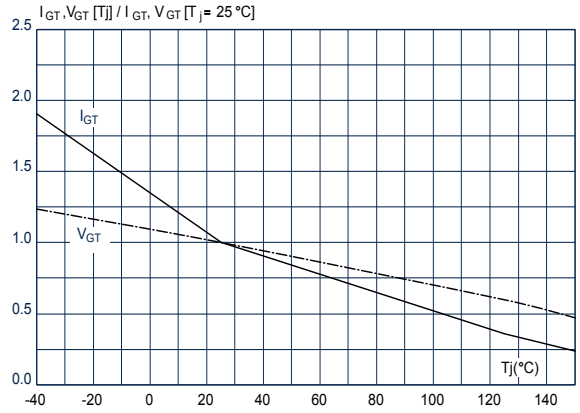


Figure 9. Relative variation of gate triggering current and voltage versus junction temperature (typical values)

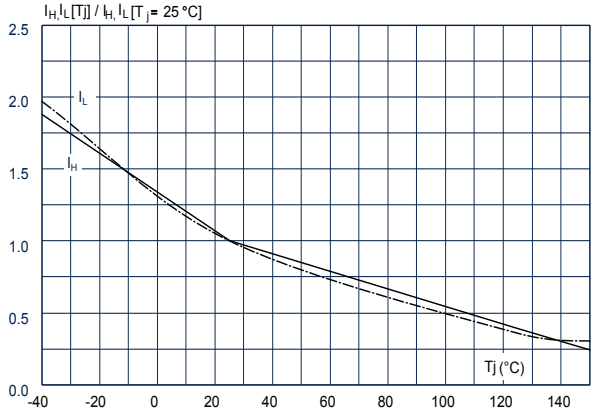


Figure 10. Relative variation of static dV/dt immunity versus junction temperature (typical values)

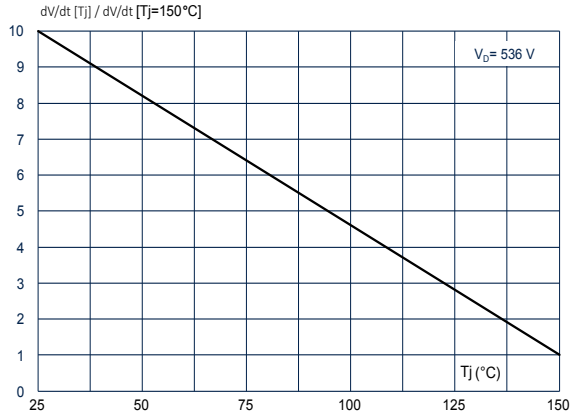


Figure 11. Relative variation of leakage current versus junction temperature for 800 V blocking voltage

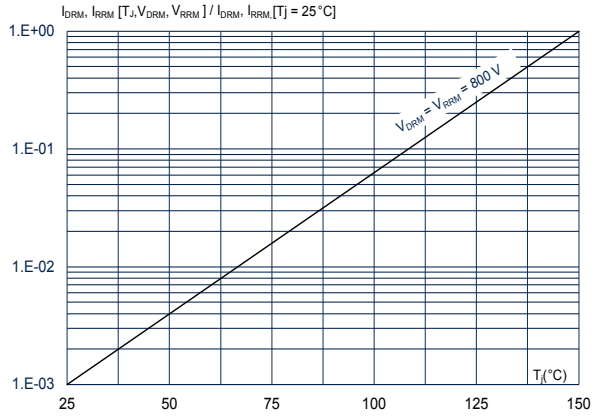


Figure 12. Thermal resistance junction to ambient versus copper surface under tab (typical values, epoxy printed board FR4, e_{Cu}= 70 µm)

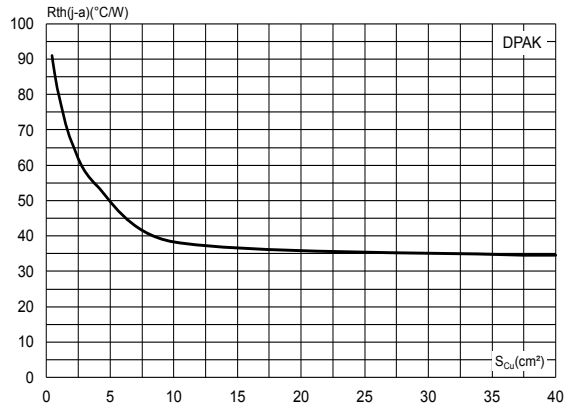


Figure 13. Relative variation of T_q versus junction temperature for different dv/dt reapplied

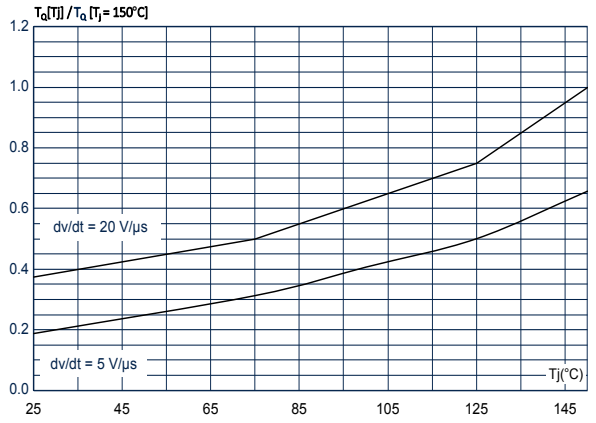


Figure 14. Relative variation of T_q versus dv/dt reapplied

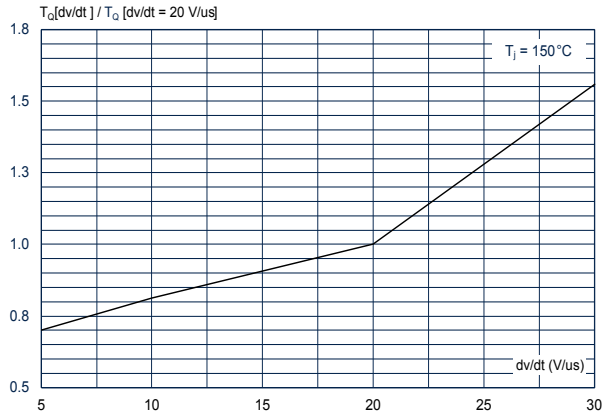
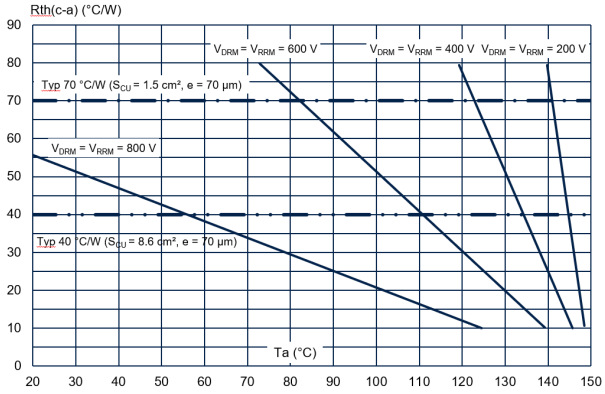


Figure 15. Recommended maximum case-to-ambient thermal resistance versus ambient temperature for different peak off-state voltages (for heatsink sizing to avoid thermal runaway)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 DPAK package information

- Molding compounded resin is halogen free and meets UL94 flammability standard, level V0
- Lead-free package leads plating

Figure 16. DPAK package outline

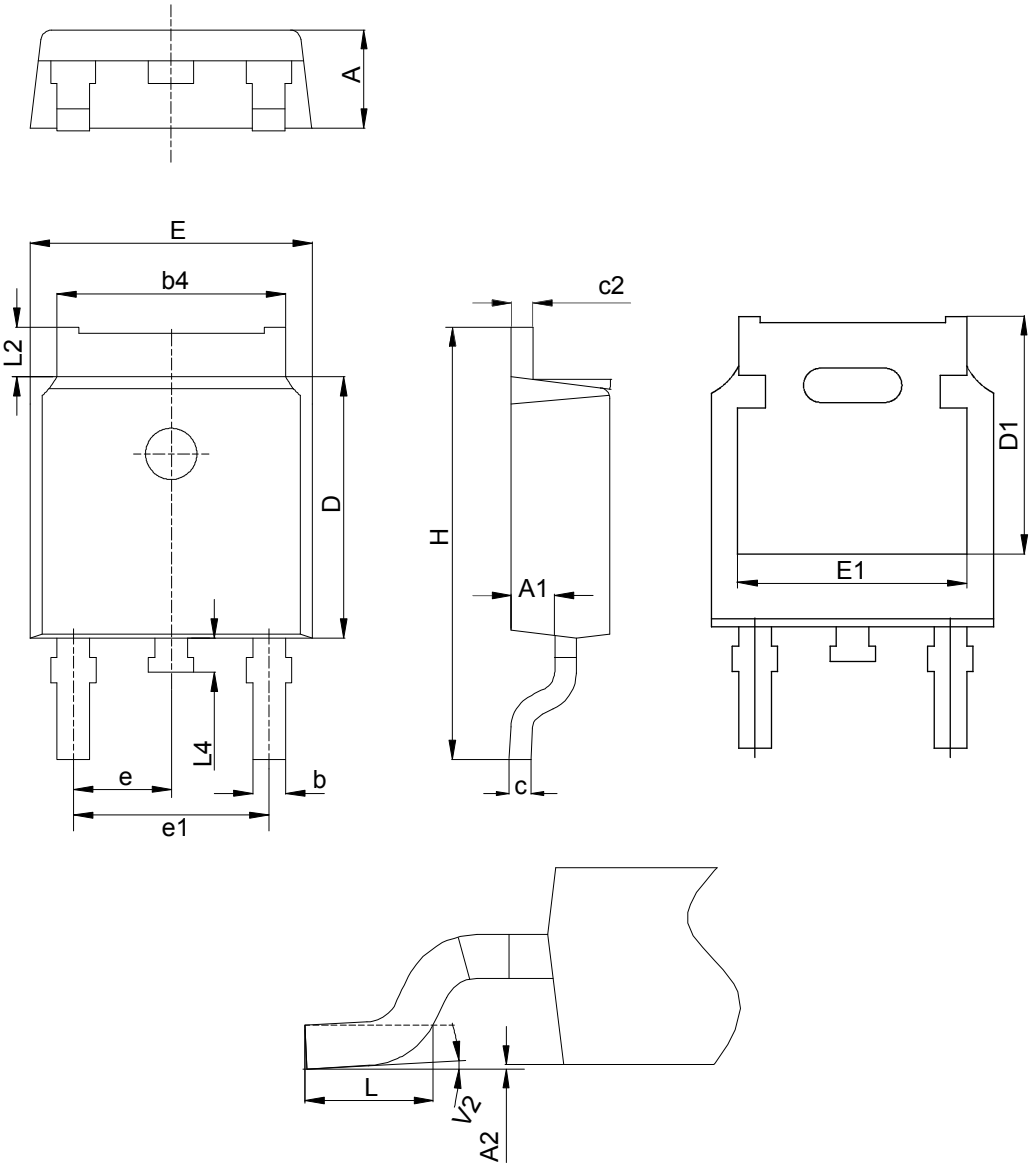


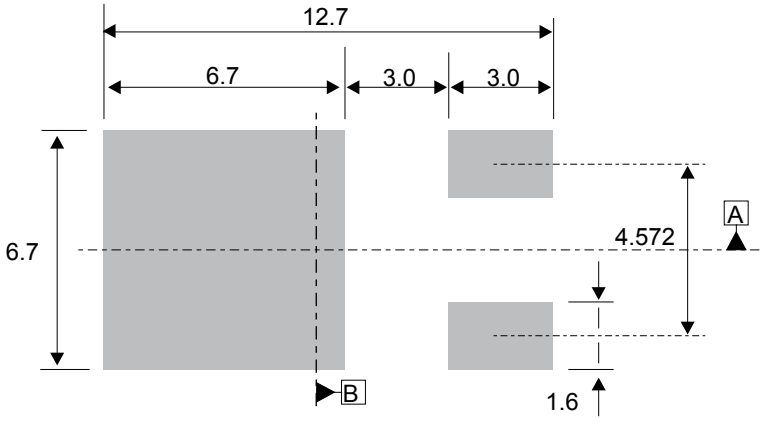
Table 5. DPAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18		2.40	0.0858		0.0945
A1	0.90		1.10	0.0354		0.0433
A2	0.03		0.23	0.0012		0.0091
b	0.64		0.90	0.0252		0.354
b4	4.95		5.46	0.1949		0.2150
c	0.46		0.61	0.0181		0.0240
c2	0.46		0.60	0.0181		0.0236
D	5.97		6.22	0.2350		0.2449
D1	4.95		5.60	0.1949		0.2205
E	6.35		6.73	0.2500		0.2650
E1	4.32		5.50	0.1701		0.2165
e		2.286			0.0900	
e1	4.40		4.70	0.1732		0.1850
H	9.35		10.40	0.3681		0.4094
L	1.00		1.78	0.0394		0.0701
L2			1.27			0.0500
L4	0.60		1.02	0.0236		0.0402
V2[2]	-8°		+8°	-8°		+8°

1. *Dimensions in inches are given for reference only*
2. *Degree*

Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

Figure 17. DPAK recommended footprint (dimensions are in mm)



The device must be positioned within ⌖ 0.05 A B

3 Ordering information

Figure 18. **Ordering information scheme**

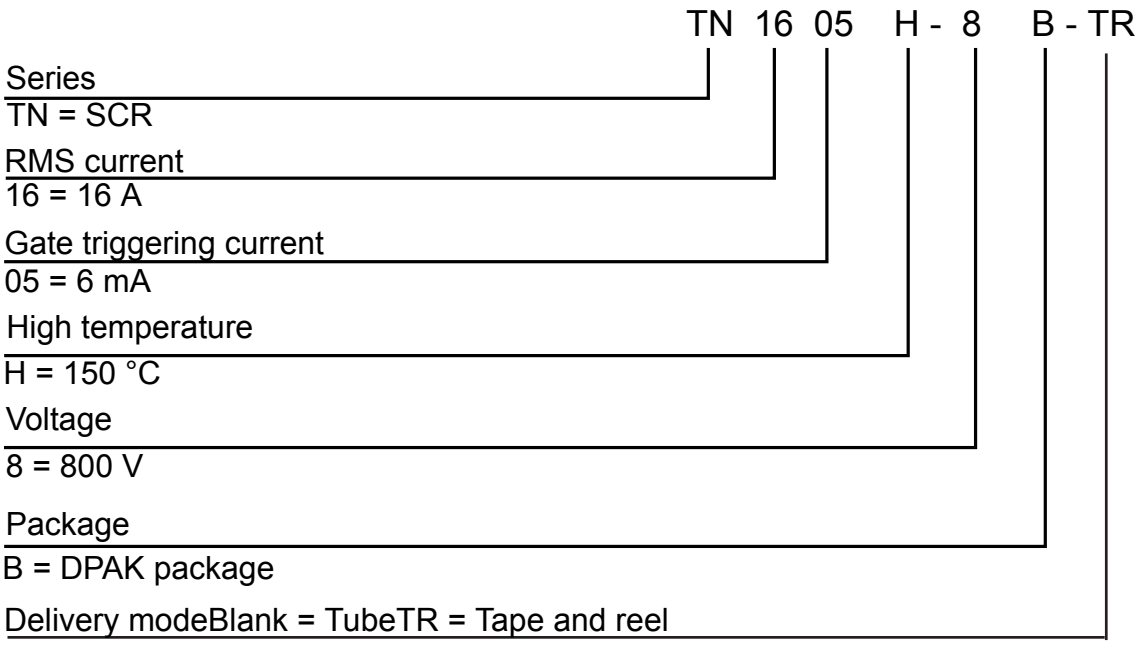


Table 6. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN1605H-8B	TN1605H8B	DPAK	0.35 g	2500	Tape and reel

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
07-Jul-2023	1	Initial release.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.