

CSD16570Q5B 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Extremely Low Resistance
- Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

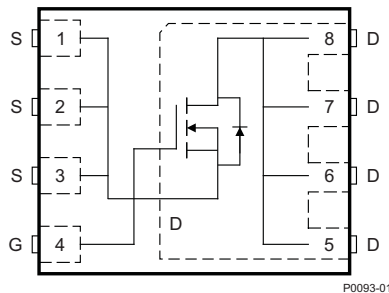
2 Applications

- ORing and Hot Swap Applications

3 Description

This 25 V, 0.49 mΩ, SON 5 × 6 mm NexFET™ power MOSFET is designed to minimize resistance for ORing and hot swap applications and is not designed for switching applications.

Top Icon



P0093-01

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	95		nC
Q_{gd}	Gate Charge Gate-to-Drain	31		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	0.68	mΩ
		$V_{GS} = 10\text{ V}$	0.49	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD16570Q5B	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD16570Q5BT	250	7-Inch Reel		

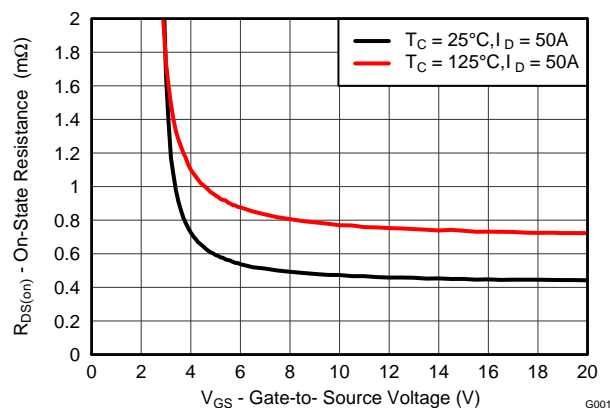
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

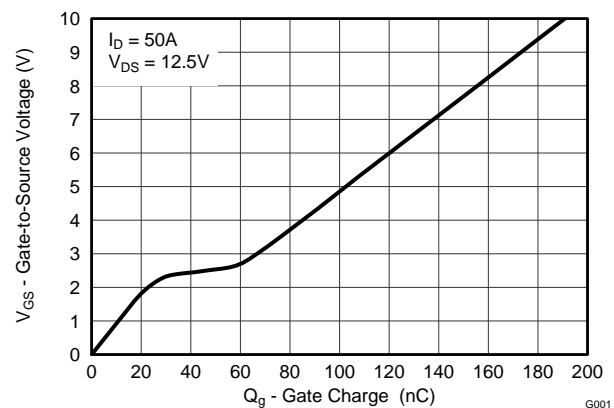
$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	456	
	Continuous Drain Current ⁽¹⁾	59	
I_{DM}	Pulsed Drain Current ⁽²⁾	400	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	195	
T_J , T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 98\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	480	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 0.8^\circ\text{C/W}$, Pulse duration ≤ 100 μs, duty cycle ≤ 1%

 $R_{DS(on)}$ vs V_{GS} 

G001

Gate Charge

G001



Table of Contents

1 Features	1	6.2 Community Resources.....	7
2 Applications	1	6.3 Trademarks	7
3 Description	1	6.4 Electrostatic Discharge Caution	7
4 Revision History	2	6.5 Glossary	7
5 Specifications	3	7 Mechanical, Packaging, and Orderable Information	8
5.1 Electrical Characteristics.....	3	7.1 Q5B Package Dimensions	8
5.2 Thermal Information	3	7.2 Recommended PCB Pattern.....	9
5.3 Typical MOSFET Characteristics.....	4	7.3 Recommended Stencil Pattern	9
6 Device and Documentation Support	7	7.4 Q5B Tape and Reel Information	10
6.1 Receiving Notification of Documentation Updates....	7		

4 Revision History

Changes from Original (July 2014) to Revision A	Page
• Added the <i>Receiving Notification of Documentation Updates</i> and <i>Community Resource</i> sections to <i>Device and Documentation Support</i>	7
• Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the <i>Recommended PCB Pattern</i> section diagram.....	9

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	25			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.1	1.5	1.9	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _D = 50 A	0.68		0.82	mΩ
		V _{GS} = 10 V, I _D = 50 A	0.49		0.59	mΩ
g _{fs}	Transconductance	V _{DS} = 2.5 V, I _D = 50 A	278			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 12 V, f = 1 MHz	10700		14000	pF
C _{oss}	Output Capacitance		1660		2160	pF
C _{rss}	Reverse Transfer Capacitance		996		1290	pF
R _G	Series Gate Resistance		1.8		3.6	Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 12.5 V, I _D = 50 A	95		124	nC
Q _g	Gate Charge Total (10 V)		192		250	nC
Q _{gd}	Gate Charge Gate-to-Drain		31			nC
Q _{gs}	Gate Charge Gate-to-Source		29			nC
Q _{g(th)}	Gate Charge at V _{th}		15			nC
Q _{oss}	Output Charge	V _{DS} = 12.5 V, V _{GS} = 0 V	35			nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5 V, V _{GS} = 10 V, I _{DS} = 50 A, R _G = 0 Ω	5			ns
t _r	Rise Time		43			ns
t _{d(off)}	Turn Off Delay Time		156			ns
t _f	Fall Time		72			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 50 A, V _{GS} = 0 V	0.8		1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 12.5 V, I _F = 50 A, di/dt = 300A/μs	34			nC
t _{rr}	Reverse Recovery Time		21			ns

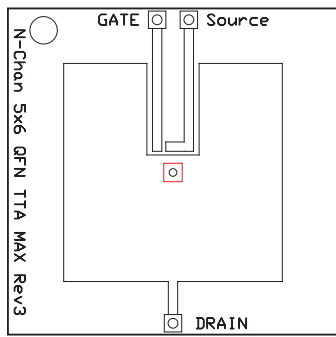
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance ⁽¹⁾			0.8	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

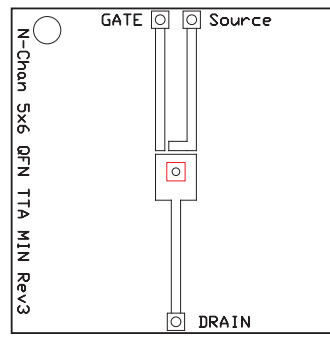
(1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
 when mounted on
 1 inch² (6.45 cm²) of
 2-oz. (0.071-mm thick)
 Cu.

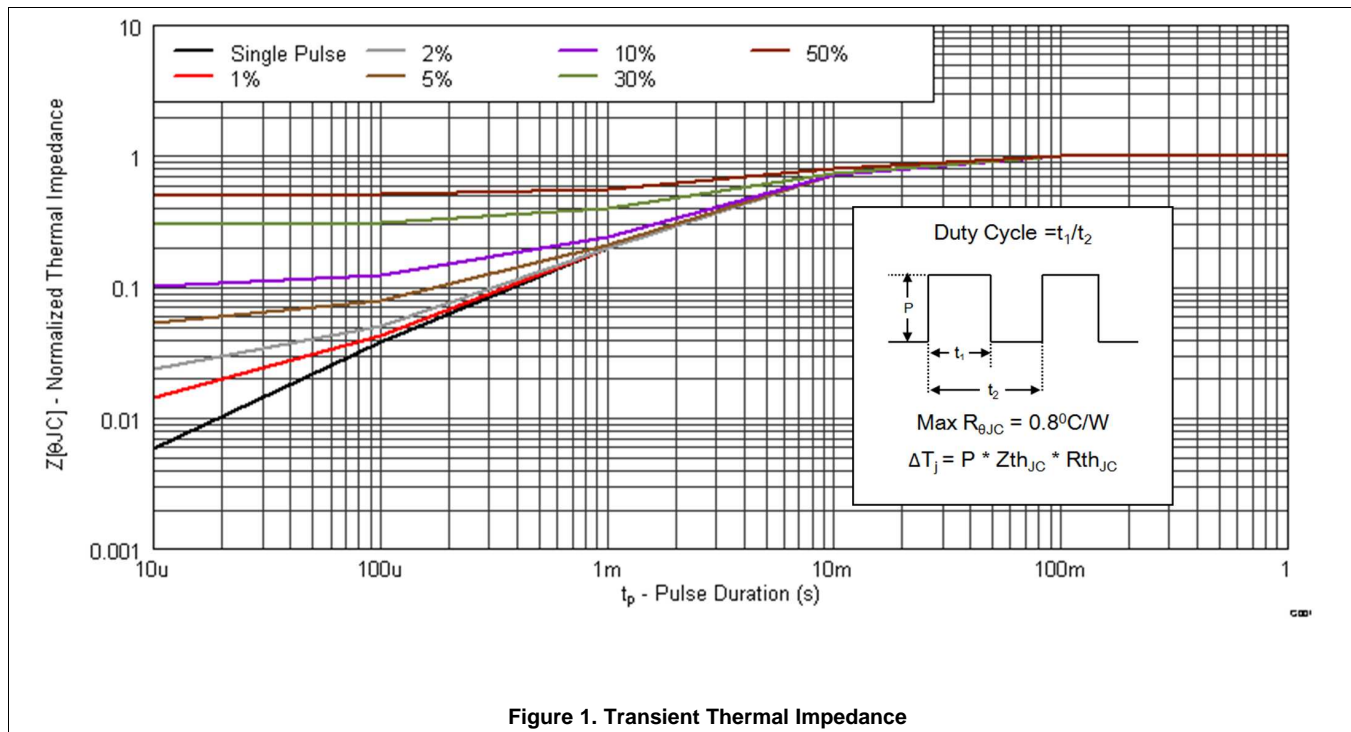


M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
 when mounted on a
 minimum pad area of
 2-oz. (0.071-mm thick)
 Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

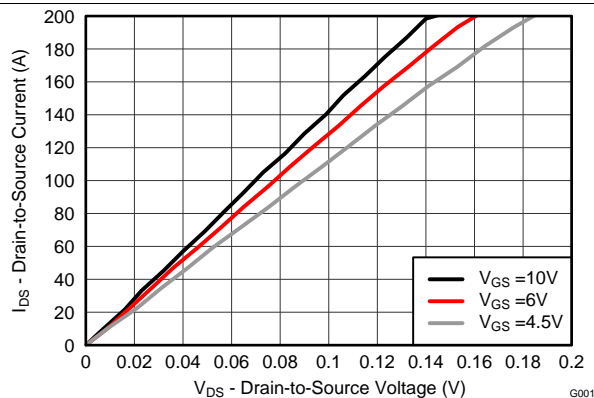


Figure 2. Saturation Characteristics

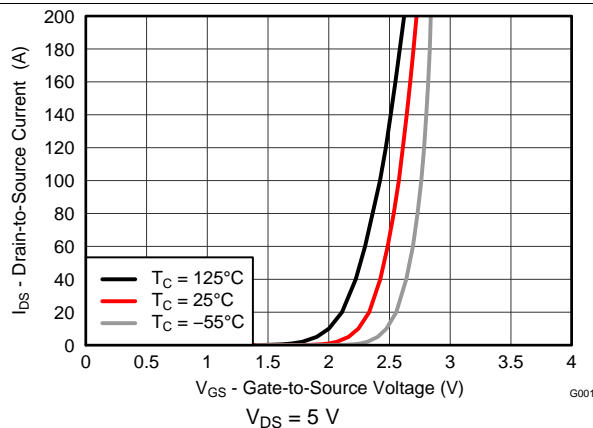


Figure 3. Transfer Characteristics

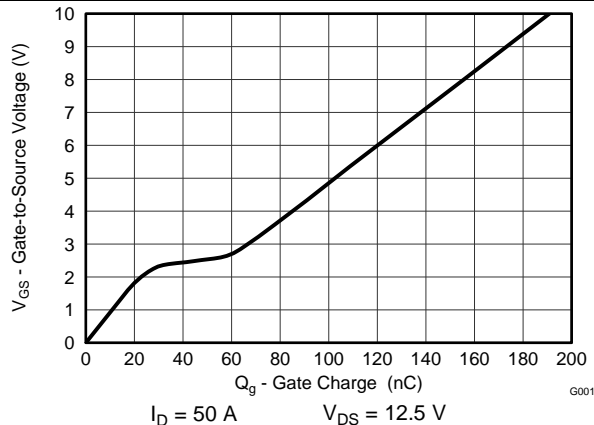


Figure 4. Gate Charge

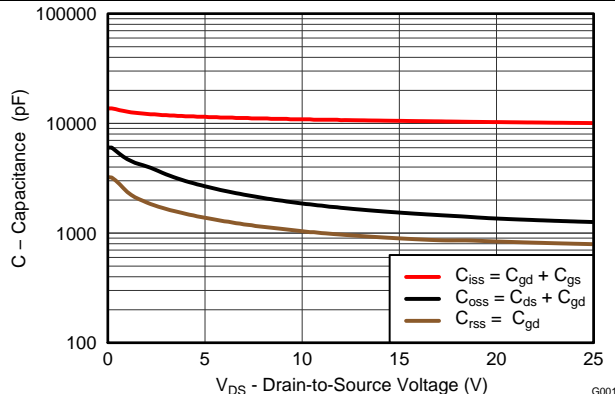


Figure 5. Capacitance

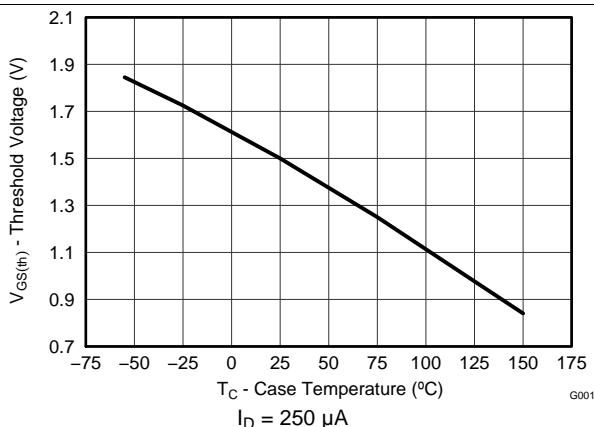


Figure 6. Threshold Voltage vs Temperature

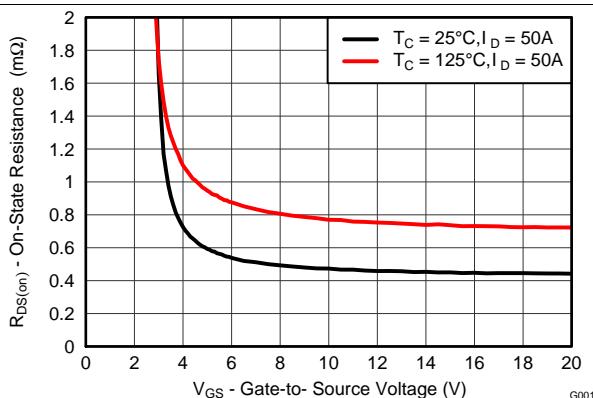


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

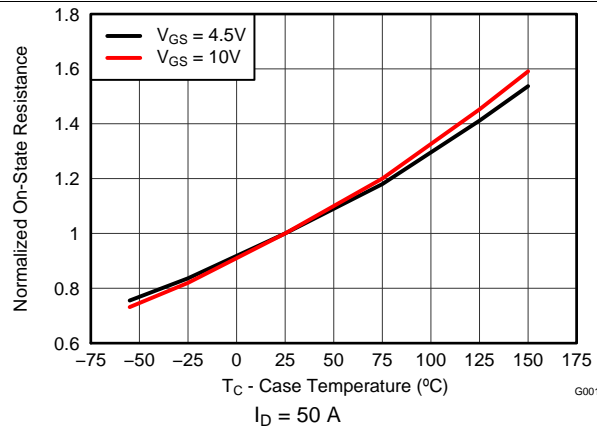


Figure 8. Normalized On-State Resistance vs Temperature

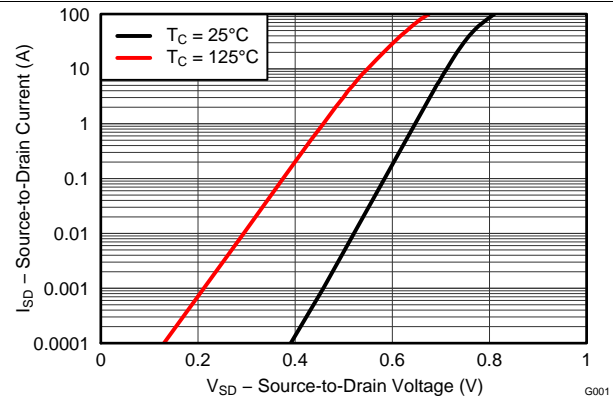


Figure 9. Typical Diode Forward Voltage

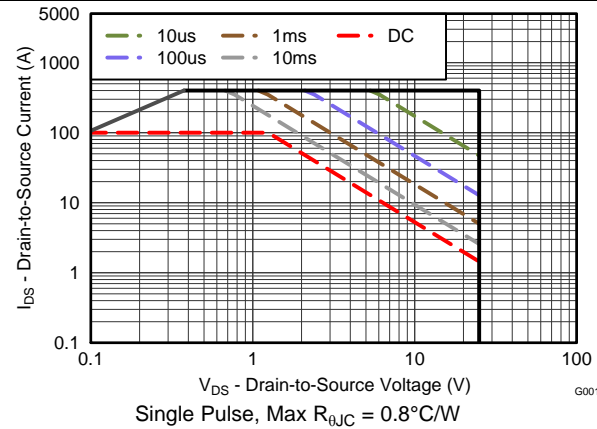


Figure 10. Maximum Safe Operating Area

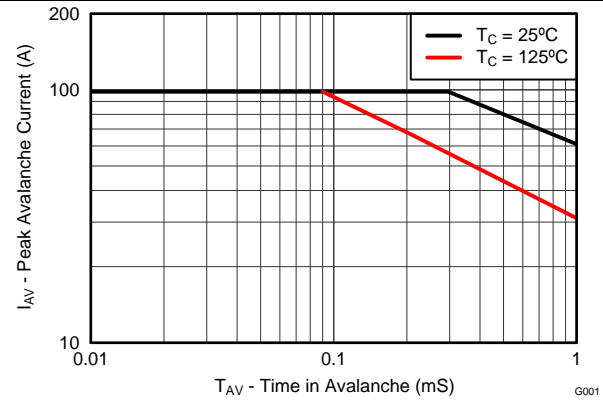


Figure 11. Single Pulse Unclamped Inductive Switching

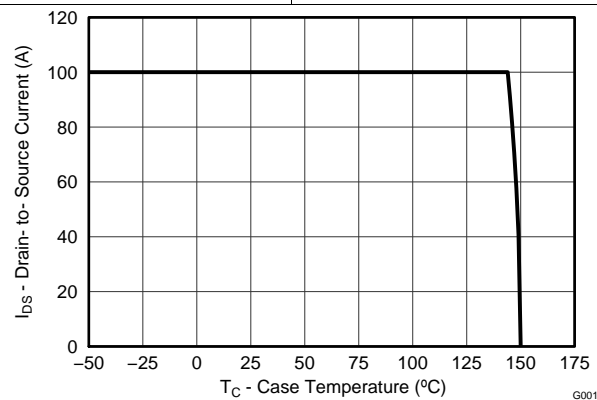


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

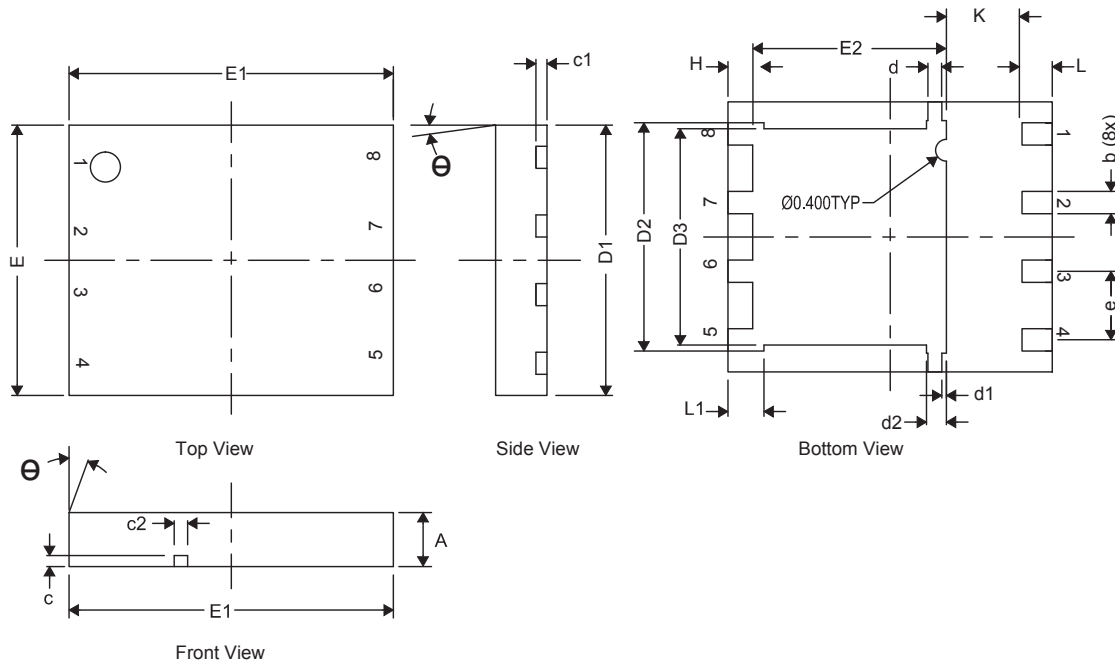
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

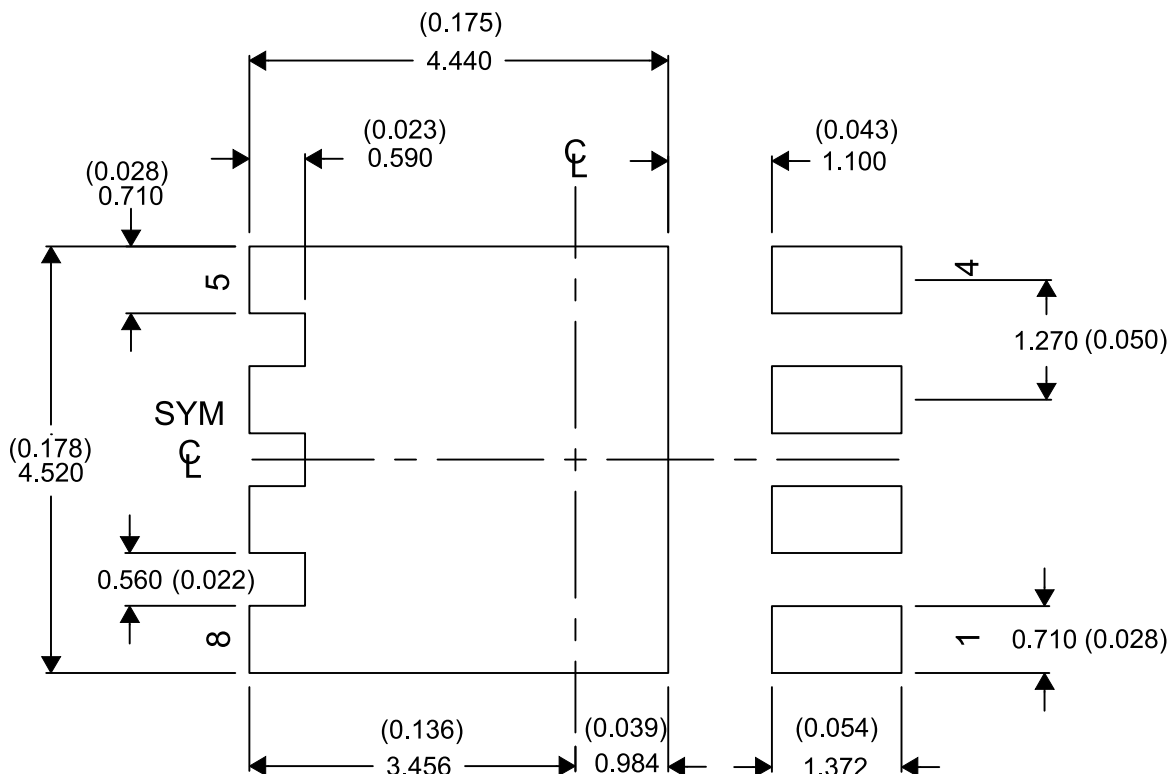
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5B Package Dimensions



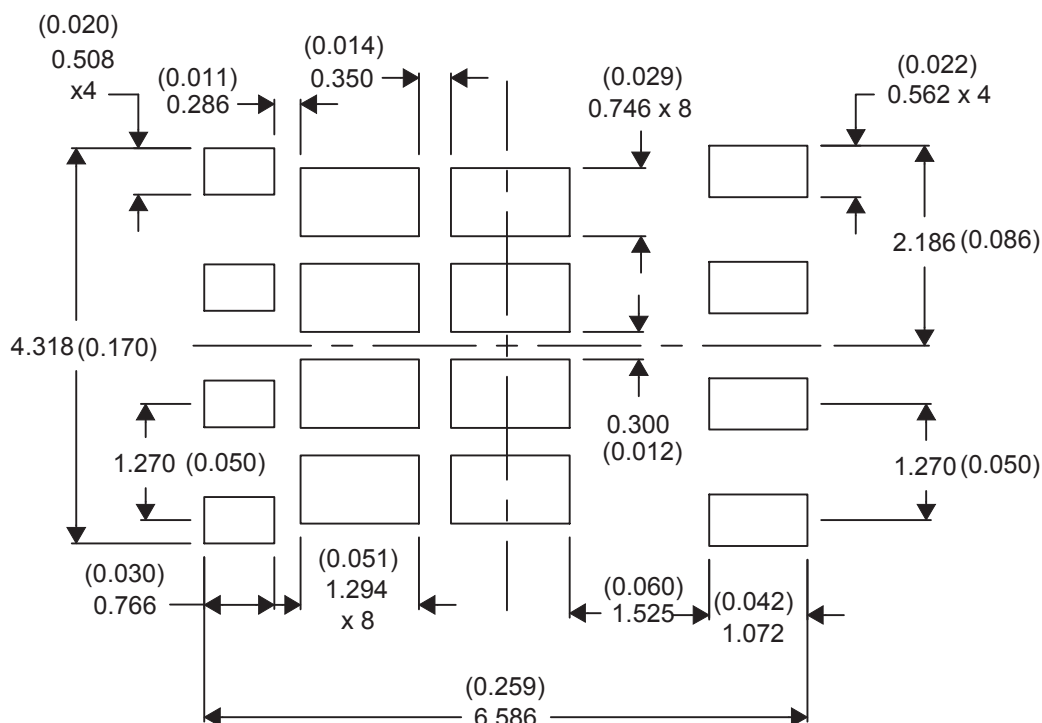
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 TYP		

7.2 Recommended PCB Pattern

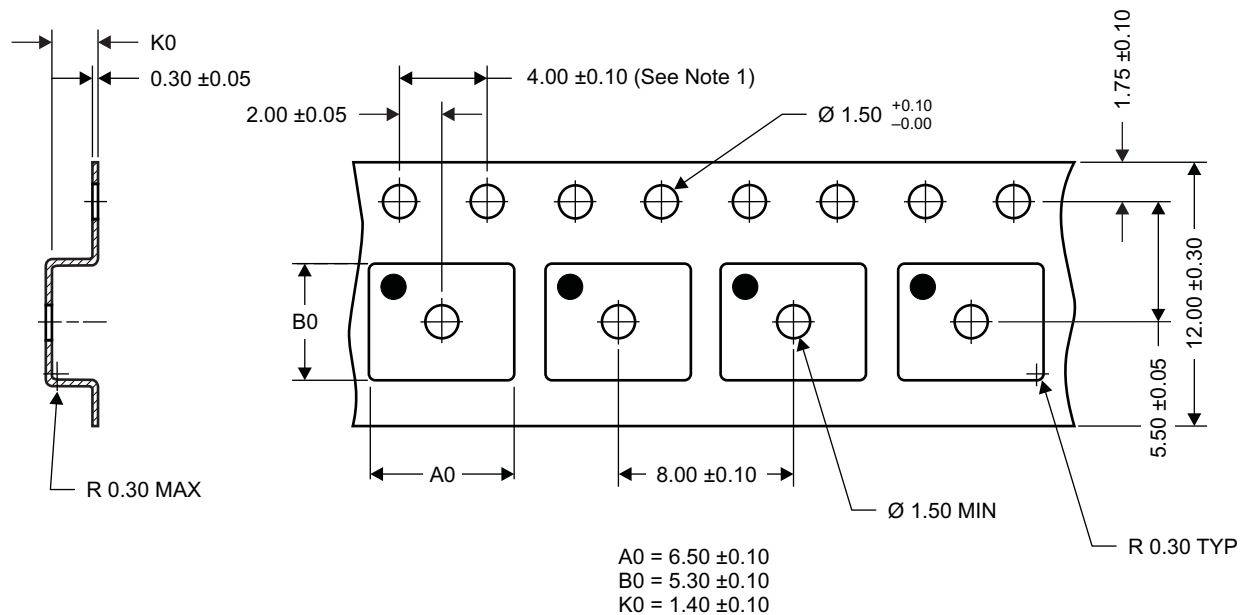


For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



M0138-01

Notes:

1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16570Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	CSD16570	Samples
CSD16570Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	CSD16570	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.