

### SPECIFICATIONS

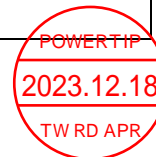
CUSTOMER	:	CES008
SAMPLE CODE	:	SH480480T001-ZHA
MASS PRODUCTION CODE	:	PH480480T001-ZHA
SAMPLE VERSION	:	01
SPECIFICATIONS EDITION	:	001
DRAWING NO. (Ver.)	:	LMD-PH480480T001-ZHA (Ver.001)
PACKAGING NO. (Ver.)	:	-

Customer Approved

Date:

Approved	Checked	Designer
廖志豪 Rex Liao	陳宗淇 Howard Chen	黃丞毅 Ian Huang

- Preliminary specification for design input
- Specification for sample approval



### POWER TIP TECH. CORP.

**Headquarters:** No.8, 6<sup>th</sup> Road, Taichung Industrial Park,  
Taichung, Taiwan  
台中市 407 工業區六路 8 號

TEL: 886-4-2355-8168

FAX: 886-4-2355-8166

E-mail: [sales@powertip.com.tw](mailto:sales@powertip.com.tw)

[Http://www.powertip.com.tw](http://www.powertip.com.tw)



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## 1. SPECIFICATIONS

### 1.1 Features

<u>Item</u>	<u>Standard Value</u>
Display Resolution	480*3(RGB)*480 Dots
LCD Type	Full Viewing Angle , Normally Black , Transmissive Type
Screen size(inch)	4 inch
Color configuration	R.G.B. Vertical Stripe
Weight	-
Interface	16/18/24 Bit RGB + 3-Line SPI (Setup)
Driver IC	ST7701S
ROHS	THIS PRODUCT CONFORMS THE ROHS OF PTC Detail information please refer website: <a href="http://www.powertip.com.tw/news_detail.php?Key=1&amp;clD=1">http://www.powertip.com.tw/news_detail.php?Key=1&amp;clD=1</a>

### 1.2 Mechanical Specifications

<u>Item</u>	<u>Standard Value</u>	<u>Unit</u>
Outline Dimension	77.0 (W) * 80.0 (L) * 2.3 (H)	mm

#### LCD Panel

<u>Item</u>	<u>Standard Value</u>	<u>Unit</u>
Active Area	71.856 (W) * 70.176 (L)	mm

Note: For detailed information please refer to LCM drawing.

### 1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	VDD		-0.3	+4.6	V
Supply Voltage (Logic)	VDDI		-0.3	+4.6	V
Operating Temperature	T <sub>OP</sub> (Ts)	Note 1	-30	+85	°C
Storage Temperature	T <sub>ST</sub> (Ta)	Note 2	-40	+90	°C

The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

Note 1: Ts is the temperature of panel' s surface.

Note 2: Ta is the ambient temperature of samples.

### 1.4 DC Electrical Characteristics

GND = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Supply Voltage	VDD	-	2.5	3.3	3.6	V	
Supply Voltage (Logic)	VDDI	-	1.65	1.8	3.6	V	
Input Signal Voltage	V <sub>IH</sub>	-	0.7*VDDI		VDDI	V	
	V <sub>IL</sub>	-	GND		0.3*VDDI	V	
Output Signal Voltage	V <sub>OH</sub>		0.8*VDDI		VDDI	V	
	V <sub>OL</sub>		GND		0.2*VDDI	V	
Supply Current	I <sub>DD</sub>	VDD=3.3V		(30)		mA	Note1
Supply Current (Logic)	I <sub>DDI</sub>	VDDI=1.8V		TBD		mA	

Note1:Maximum current display

## 1.5 Optical Characteristics

### TFT LCD Panel

VDD=3.3V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	-	
Response Time	Tr + Tf	-	-	25	35	ms	Note2	
Viewing Angle	Top	ΘY+	CR ≥ 10	70	80	-	Deg.	Note4
	Bottom	ΘY-		70	80	-		
	Left	ΘX-		70	80	-		
	Right	ΘX+		70	80	-		
Contrast Ratio	CR	-	640	800	-	-	Note3	
Color of CIE Coordinate (With B/L)	White	X	-	(0.30)	-	-	Note1	
		Y-	-	(0.33)	-			
	Red	X	-	(0.62)	-			
		Y	-	(0.33)	-			
	Green	X	-	(0.29)	-			
		Y	-	(0.52)	-			
	Blue	X	-	(0.14)	-			
		Y	-	(0.14)	-			
Average Brightness Pattern=White Display (With B/L)*1	IV	IF=20mA	-	(1000)	-	cd/m2	Note1	
Luminance Uniformity (With B/L)*2	Δ B	-	70	-	-	%	Note1	

Note1:

1 :  $\Delta B = B(\min) / B(\max) \times 100\%$

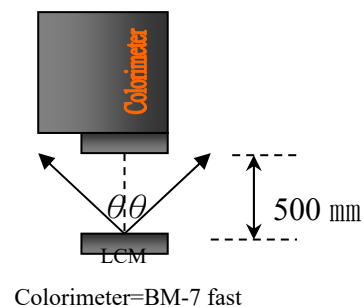
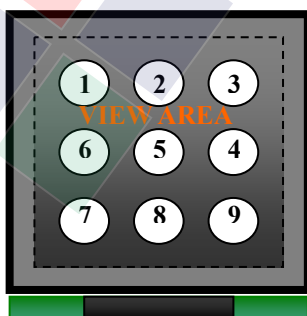
2 : Measurement Condition for Optical Characteristics:

a : Environment: 25°C±5°C / 60±20%R.H , no wind , dark room below 10 Lux at typical lamp current and typical operating frequency.

b : Measurement Distance: 500 ± 50 mm , (θ= 0°)

c : Equipment: TOPCON BM-7 fast , (field 1°) , after 10 minutes operation.

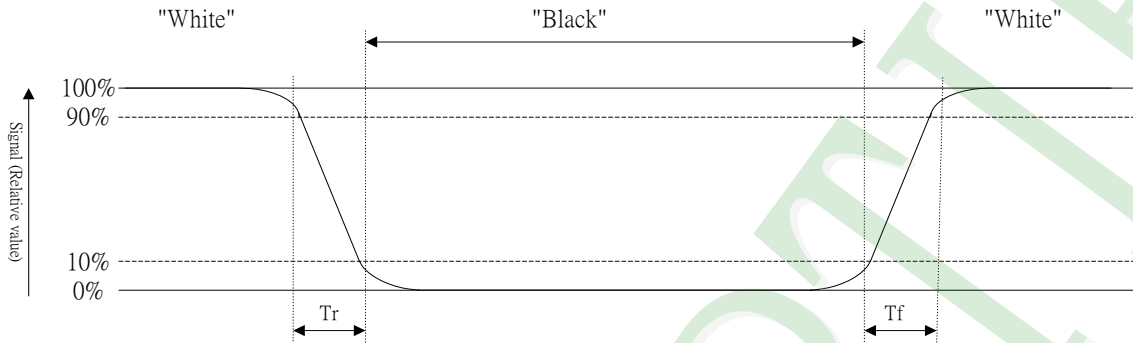
d : The uncertainty of the C.I.E coordinate measurement ±0.01 , Average Brightness ± 4%



**Note2: Definition of response time:**

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:



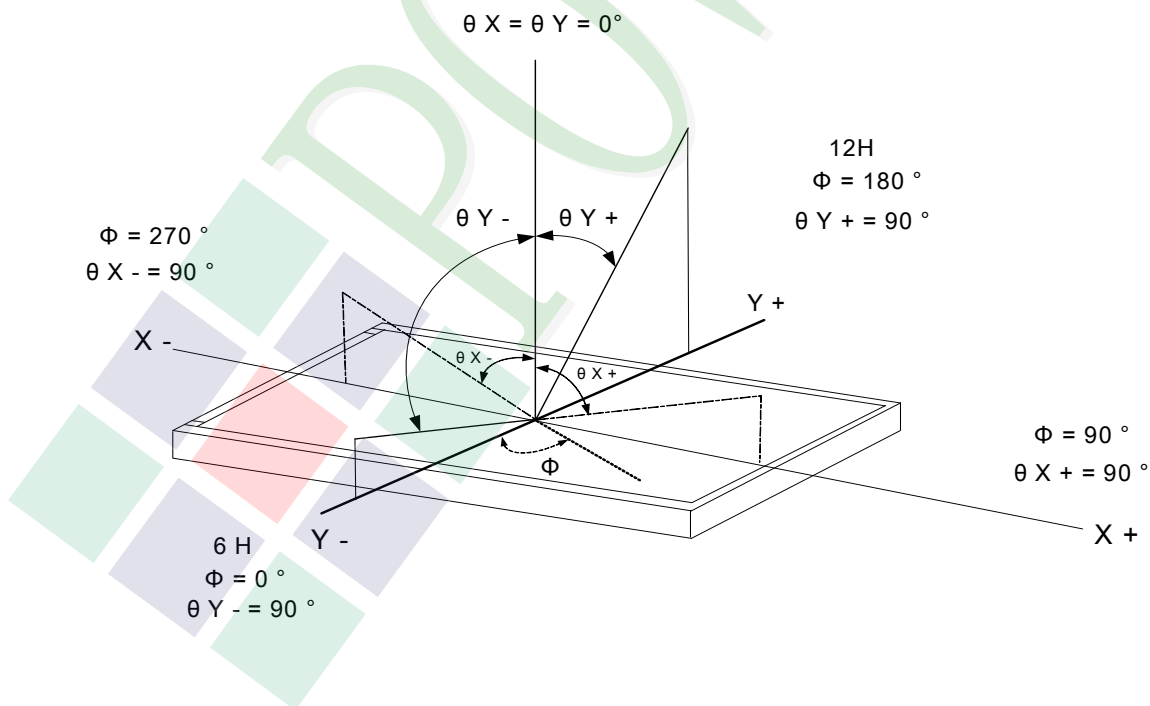
**Note3: Definition of contrast ratio:**

Contrast ratio is calculated with the following formula

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

**Note4: Definition of viewing angle:**

Refer to figure as below:



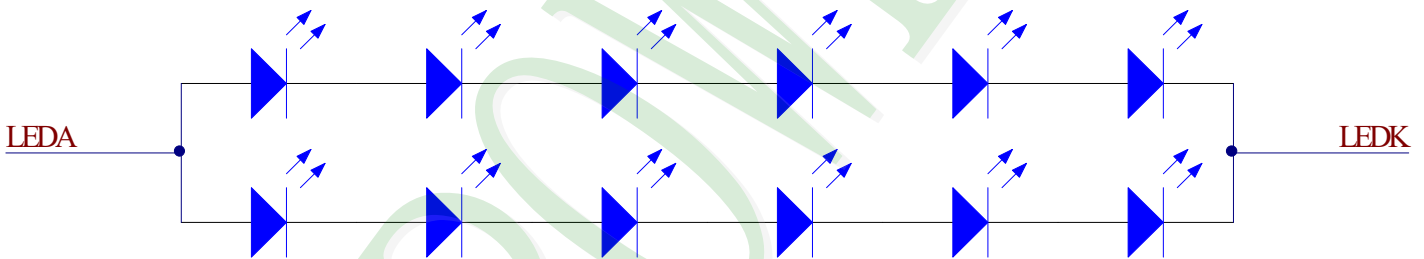
## 1.6 Backlight Characteristics

### Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
LED Forward Current	IF	Ta =25°C	-	TBD	mA
LED Reverse Voltage	VR	Ta =25°C	-	TBD	V
Power Dissipation	PD	Ta =25°C	-	TBD	W

### Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	VF	IF=20mA		(18.6)		V
Average Brightness (Without LCD )	IV			TBD		cd/m <sup>2</sup>
CIE Color Coordinate (Without LCD )	X			TBD		-
	Y			TBD		
Color		White				



### Other Description

Item	Conditions	Description
Life Time	Ta =25°C IF=200mA	50000 hrs



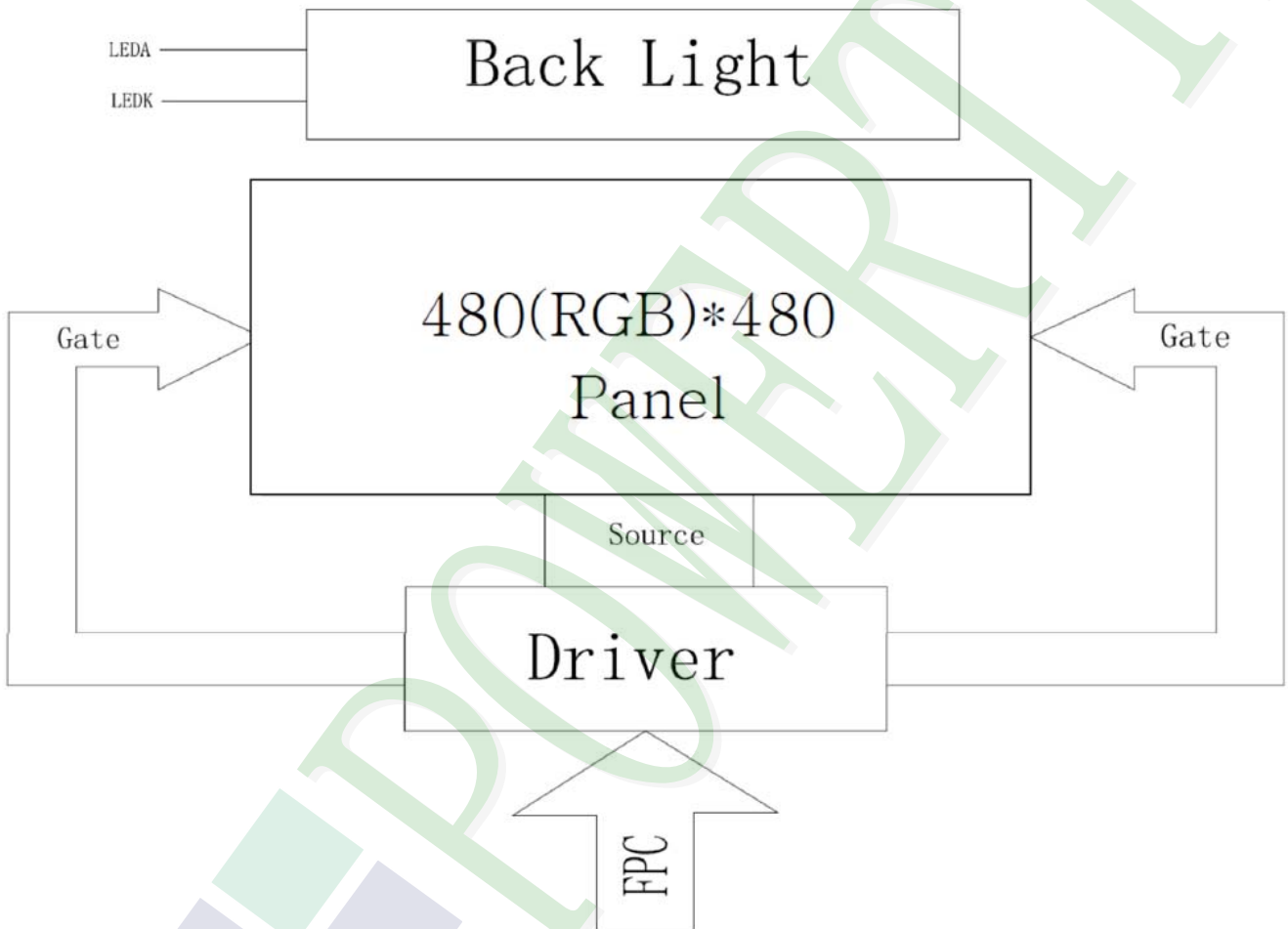
## 2. MODULE STRUCTURE

### 2.1 Counter Drawing

#### 2.1.1 LCM Mechanical Diagram

\* See Appendix

#### 2.1.2 Block Diagram



## 2.2 Interface Pin Description

### TFT LCM Interface

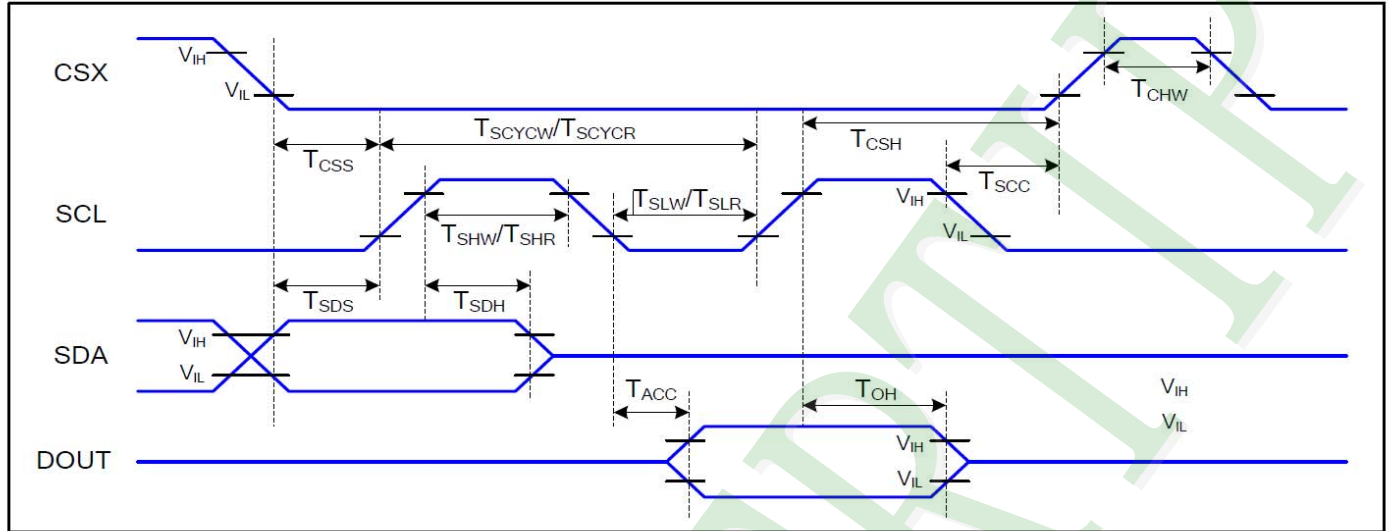
Pin No.	Symbol	Function
1	NC	No connection
2	NC	No connection
3	NC	No connection
4	NC	No connection
5	GND	Ground
6	GND	Ground
7	VDD	Supply Voltage
8	VDDI	Logic Supply Voltage
9	SDO	Serial data output pin used for the SPI Interface. Leave the pin open when not in use.
10	SDA	Serial data input pin for SPI Interface. Fix to GND level when not in use.
11	SCL	Serial clock input for SPI interface. Fix to IOVCC or GND level when not in use.
12	CSX	Chip select signal. Low: The chip is accessible High: The chip is not selected Fix to IOVCC or GND level when not in use.
13	RESET	External reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
14	DB23(R7)	Red Data.
15	DB22(R6)	Red Data.
16	DB21(R5)	Red Data.
17	DB20(R4)	Red Data.
18	DB19(R3)	Red Data.
19	DB18(R2)	Red Data.
20	DB17(R1)	Red Data.
21	DB16(R0)	Red Data.

<u>Pin No.</u>	<u>Symbol</u>	<u>Function</u>
22	DB15(G7)	Green Data.
23	DB14(G6)	Green Data.
24	DB13(G5)	Green Data.
25	DB12(G4)	Green Data.
26	DB11(G3)	Green Data.
27	DB10(G2)	Green Data.
28	DB9(G1)	Green Data.
29	DB8(G0)	Green Data.
30	DB7(B7)	Blue Data.
31	DB6(B6)	Blue Data.
32	DB5(B5)	Blue Data.
33	DB4(B4)	Blue Data.
34	DB3(B3)	Blue Data.
35	DB2(B2)	Blue Data.
36	DB1(B1)	Blue Data.
37	DB0(B0)	Blue Data.
38	DE	Data enable signal for RGB interface operation Low: access enabled High: access inhibited Fix to IOVCC or GND level when not in use.
39	PCLK	Dot clock signal for RGB interface operation Fix to IOVCC or GND level when not in use.
40	HSYNC	Line synchronizing signal for RGB interface operation Fix to IOVCC or GND level when not in use,
41	VSYNC	Frame synchronizing signal for RGB interface operation Fix to IOVCC or GND level when not in use.
42	NC	No connection
43	LEDK	LED Cathode.
44	NC	No connection
45	LEDA	LED Anode.

## 2.3 Timing Characteristics

### 2.3.1 Serial Interface Characteristics (3-line serial):

#### 3-line serial Interface Timing Characteristics

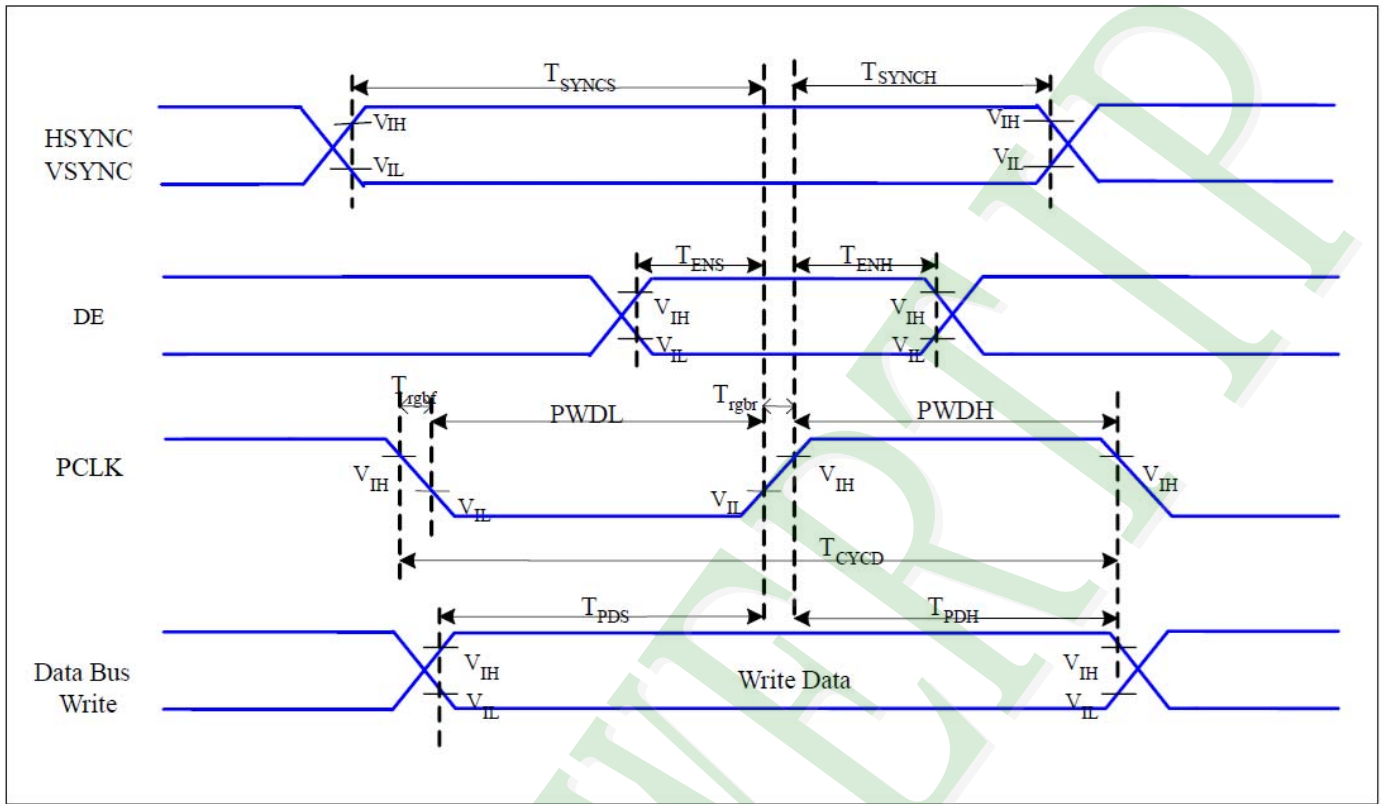


VDDI=1.8, VDD=2.8, GND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	$T_{CSS}$	Chip select setup time (write)	15		ns	
	$T_{CSH}$	Chip select hold time (write)	15		ns	
	$T_{CSS}$	Chip select setup time (read)	60		ns	
	$T_{SCC}$	Chip select hold time (read)	60		ns	
	$T_{CHW}$	Chip select "H" pulse width	40		ns	
SCL	$T_{SCYCW}$	Serial clock cycle (Write)	66		ns	
	$T_{SHW}$	SCL "H" pulse width (Write)	15		ns	
	$T_{SLW}$	SCL "L" pulse width (Write)	15		ns	
	$T_{SCYCR}$	Serial clock cycle (Read)	150		ns	
	$T_{SHR}$	SCL "H" pulse width (Read)	60		ns	
	$T_{SLR}$	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	$T_{SDS}$	Data setup time	10		ns	
	$T_{SDH}$	Data hold time	10		ns	
SDO (DOUT)	$T_{ACC}$	Access time	20	50	ns	Max: CL=30pF
	$T_{OH}$	Output disable time	50	50	ns	Min: CL=8pF

Note : The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

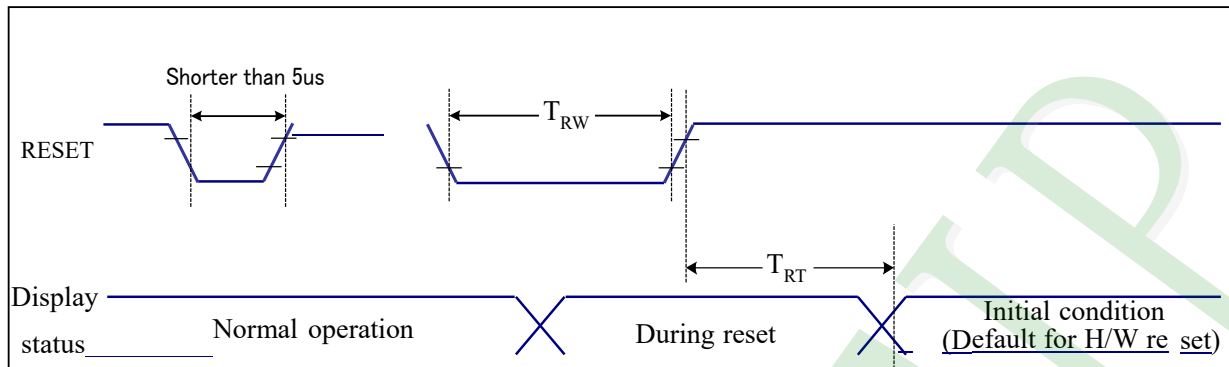
### 2.3.2 RGB Interface Characteristics :



VDDI=1.8, VDD=2.8, GND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	$T_{SYNCS}$	VSYNC, HSYNC Setup Time	5	-	ns	
DE	$T_{ENS}$	Enable Setup Time	5	-	ns	
	$T_{ENH}$	Enable Hold Time	5	-	ns	
PCLK	PWDH	PCLK High-level Pulse Width	15	-	ns	
	PWDL	PCLK Low-level Pulse Width	15	-	ns	
	$T_{CYCD}$	PCLK Cycle Time	33	-	ns	
	Trghr, Trghf	PCLK Rise/Fall time	-	15	ns	
DB	$T_{PDS}$	PD Data Setup Time	5	-	ns	
	$T_{PDH}$	PD Data Hold Time	5	-	ns	

### 2.3.3 Reset Timing:



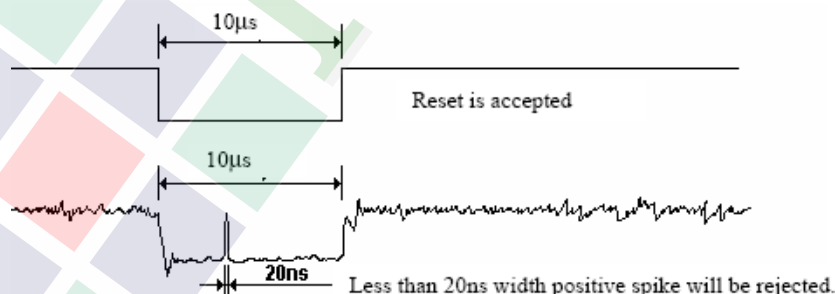
Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESET	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## RGB Interface

The ST7701SI support RGB interface Mode 1 and Mode 2. The interface signals as shown in table 6.3.1. The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701SI.

In RGB Mode 2, back porch of Vsync is defined by VBP\_HVRGB [7:0] of RGBCTR command. And back porch of Hsync is defined by HBP\_HVRGB [7:0] of RGBCTR command. Front porch of Vsync are not setting by this mode

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HSYNC	Horizontal sync	Horizontal synchronization timing signal
VSYNC	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit, 18-bit and 24-bit format

## RGB Color Format

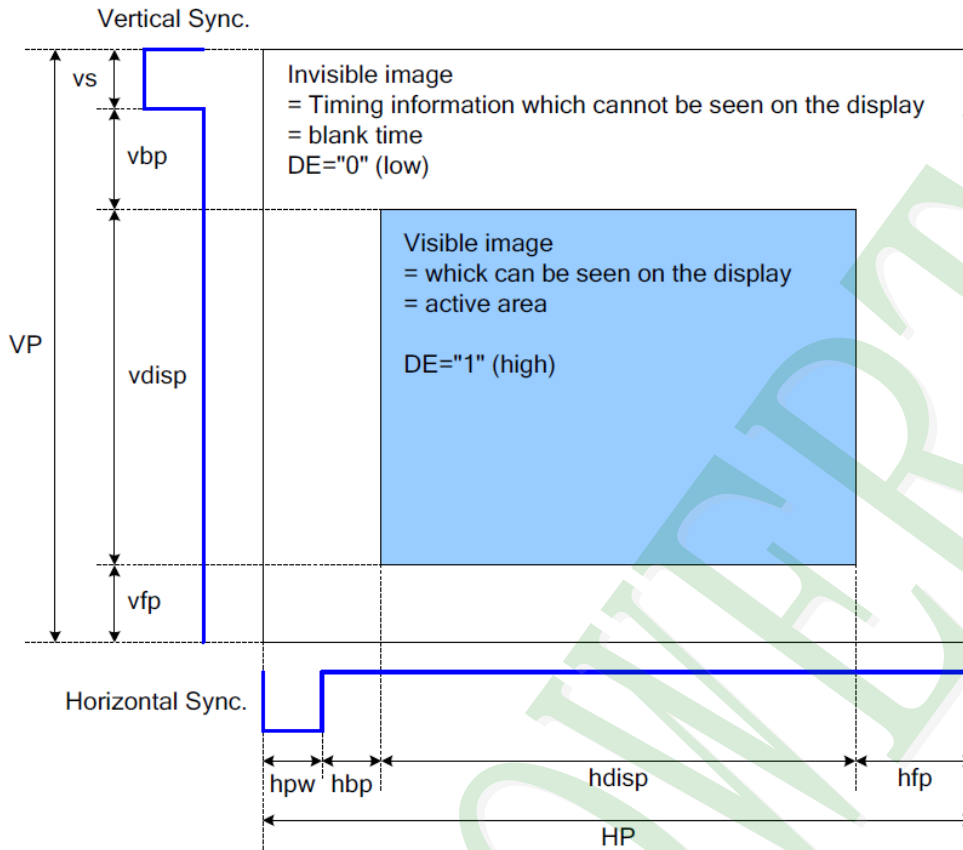
ST7701SI supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[23:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[23:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	18 bits configuration		16 bits configuration VIPF[3:0]=0101	
	24 bits configuration VIPF[3:0]=0111	VIPF[3:0]=0110		
		MDT=0		MDT=1
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0



## RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	-	255 (Note 2)	Clock
Horizontal Sync. Back Porch	hbp	2	--	255 (Note 2)	Clock
Horizontal Sync. Front Porch	hfp	2	--	-	Clock
Vertical Sync. Width	vs	2	--	254 (Note 2)	Line
Vertical Sync. Back Porch	vbp	2	--	254 (Note 2)	Line
Vertical Sync. Front Porch	vfp	2	--	--	Line

Note:

1. Typical value are related to the setting frame rate is 60Hz..
2.  $VS+VBP \leq 254$ ,  $HPW+HBP \leq 255$

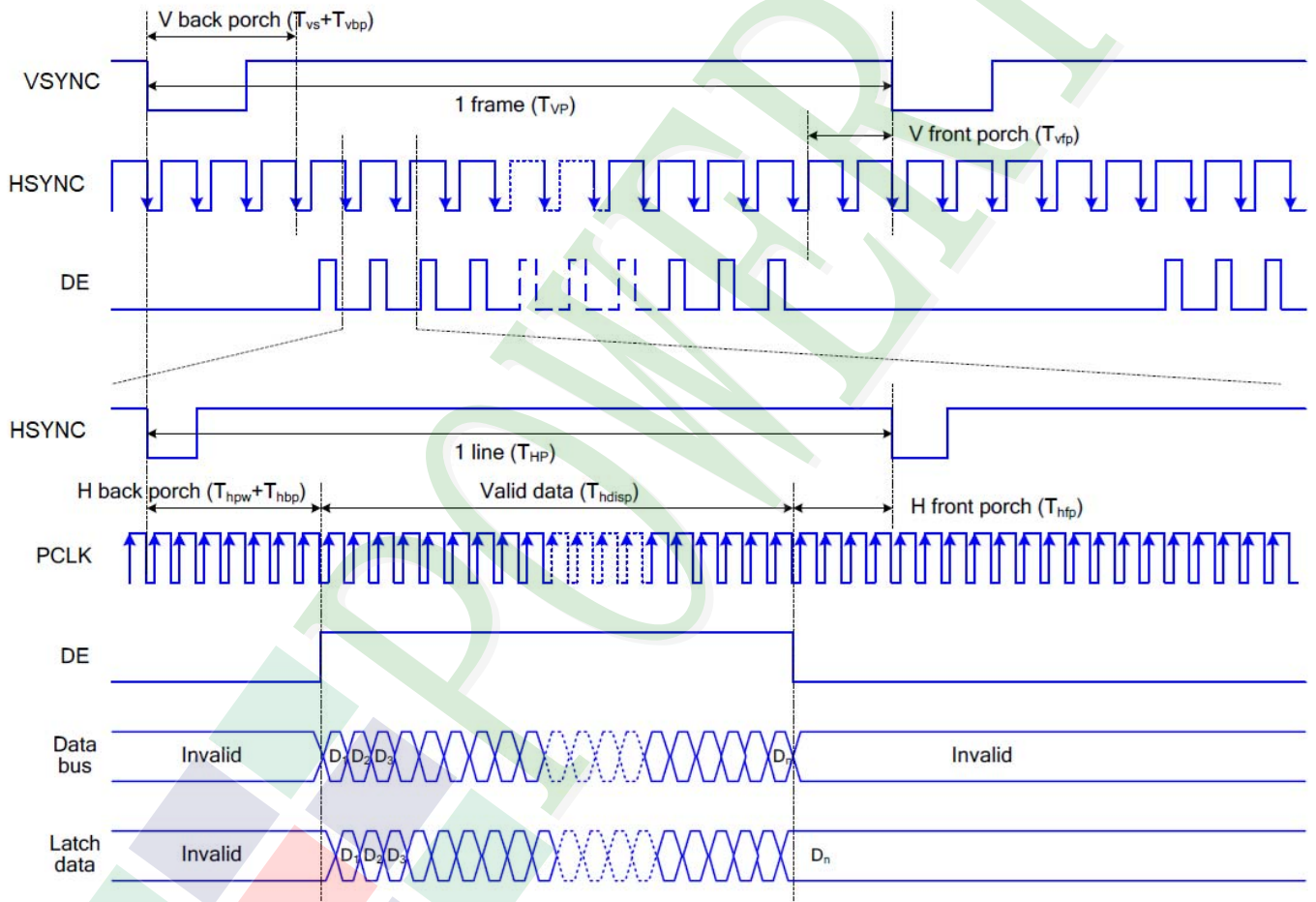
## RGB Interface Mode Selection

ST7701SI supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode
0	DE mode
1	HV mode

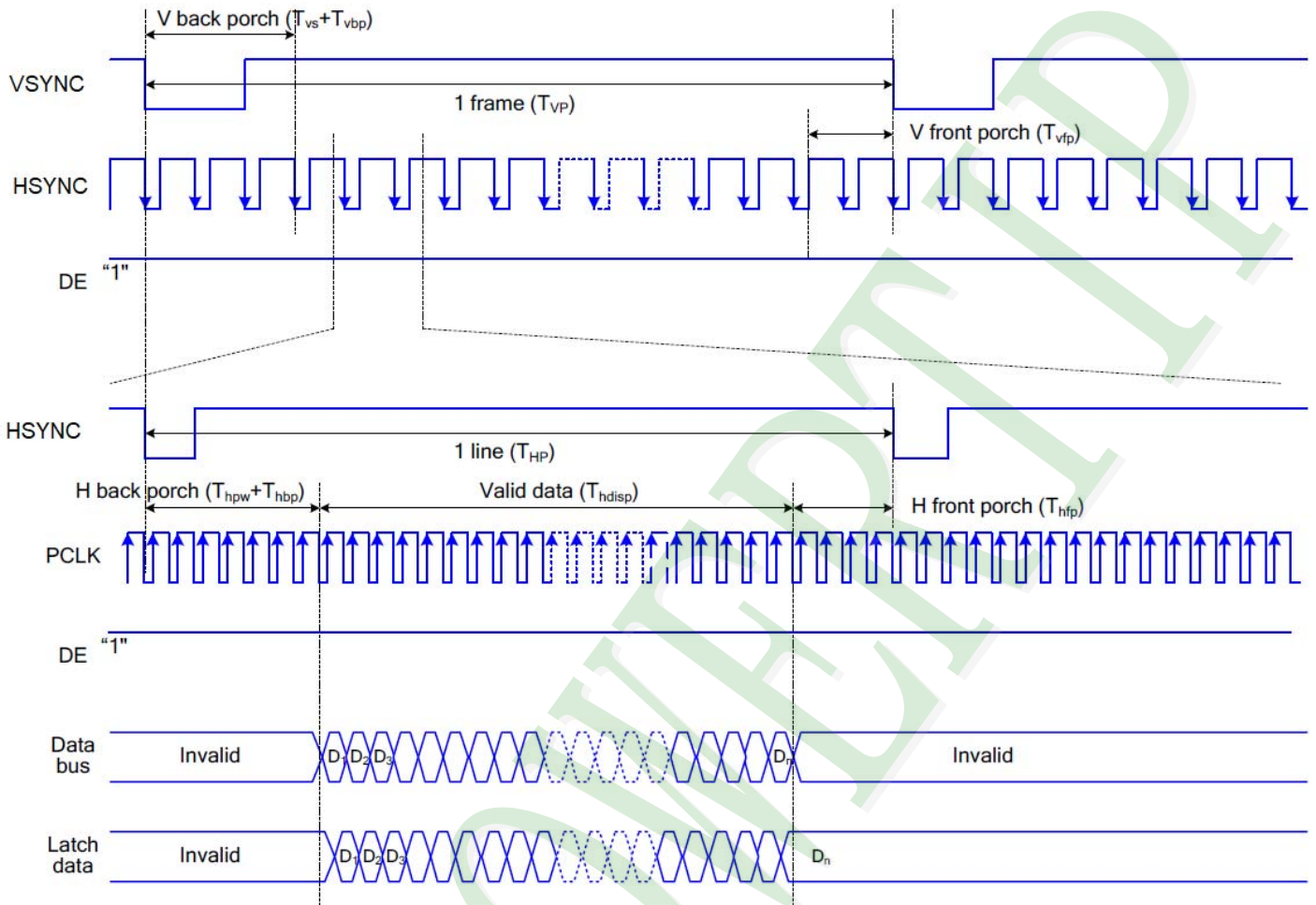
## RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



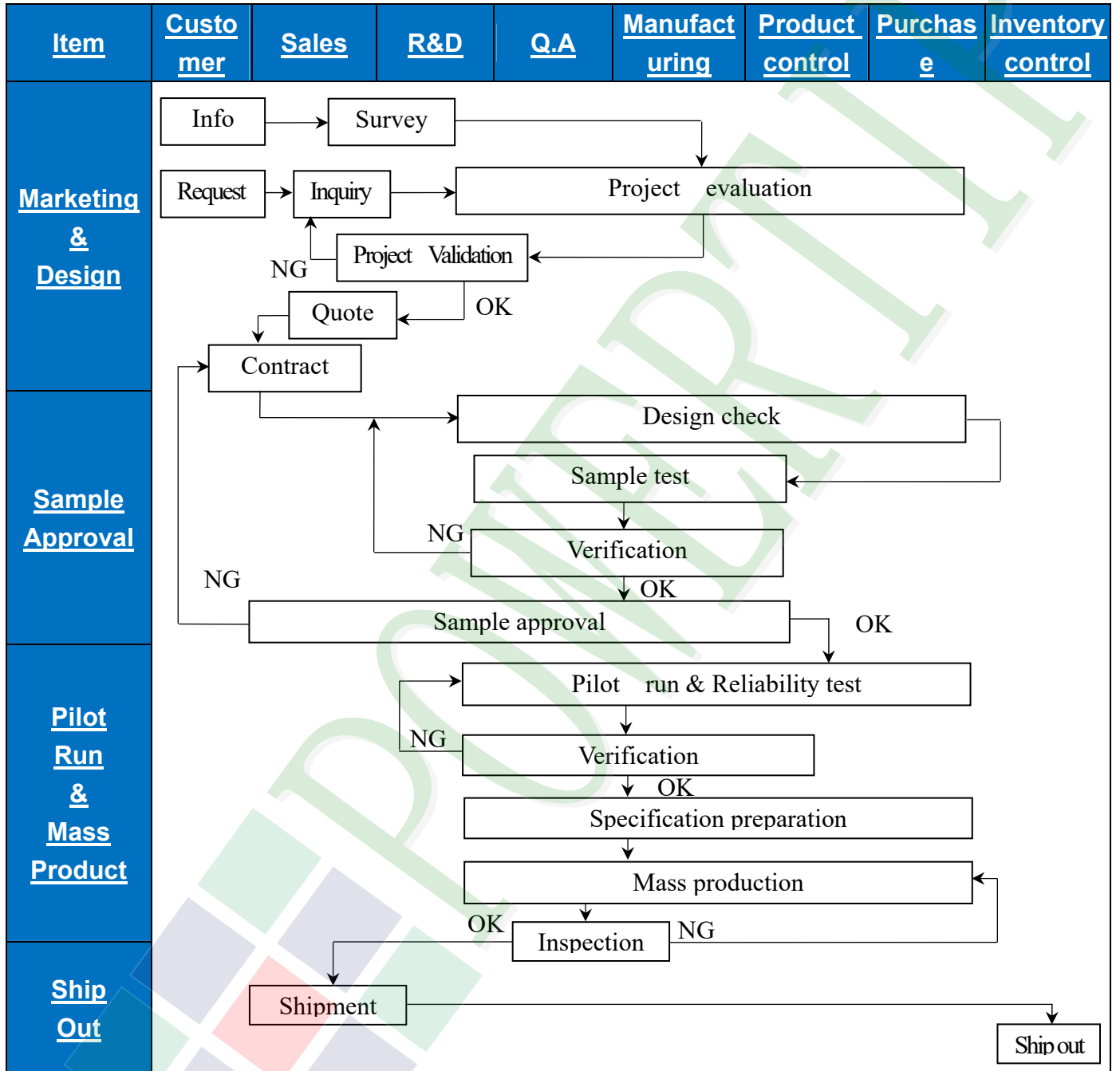
Note: The setting of front porch and back porch in host must match that in IC as this mode.

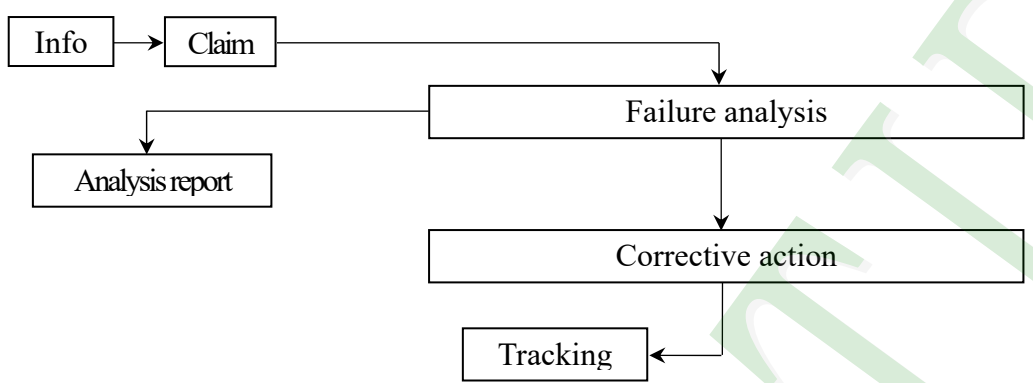
The timing chart of RGB interface HV mode is shown as follows.



### 3. QUALITY ASSURANCE SYSTEM

#### 3.1 Quality Assurance Flow Chart



<u>Item</u>	<u>Customer</u>	<u>Sales</u>	<u>R&amp;D</u>	<u>Q.A</u>	<u>Manufacturing</u>	<u>Product control</u>	<u>Purchase</u>	<u>Inventory control</u>
<u>Sales Service</u>	 <pre> graph TD     Info[Info] --&gt; Claim[Claim]     Claim --&gt; Failure[Failure analysis]     Failure --&gt; Report[Analysis report]     Failure --&gt; Action[Corrective action]     Action --&gt; Tracking[Tracking]           </pre>							
<u>Q.A Activity</u>	1. ISO 9001 Maintenance Activities 3. Equipment calibration 5. Standardization Management				2. Process improvement proposal 4. Education And Training Activities			

## 3.2. Inspection Specification

### 3.2.1 Delivery Inspection Standards

#### 3.2.1.1 Inspection Conditions

Inspection distance: 30 cm - 50cm  
Viewing angle:  $\pm 45^\circ$

#### 3.2.1.2 Environmental Conditions

Ambient temperature:  $25^\circ\text{C} \pm 5^\circ\text{C}$   
Ambient humidity:  $65 \pm 10\% \text{ RH}$   
Ambient illumination: 300~700 lux

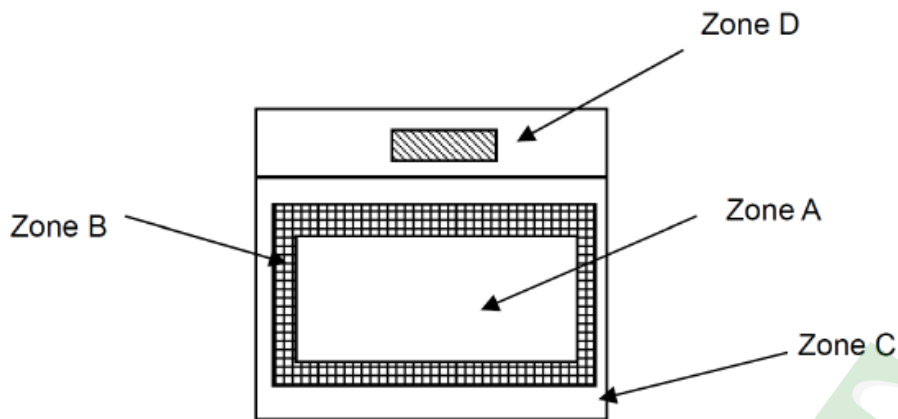
#### 3.2.1.3 Sampling Conditions

1. Lot size: quantity of shipment lot per model
2. Sampling method:

Sampling plan		GB/T 2828-2003
		Normal inspection, Class II
AQL	Major Defect	0.65%
	Minor Defect	1.5%

No.	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Colour tone	Colour unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, Polarizer bubble; Polarizer accidented spot.	
6	Soldering appearance	Good soldering, peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

### 3.2.1.4 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (ZoneA+ZoneB) which can't be seen after assembly by customer.

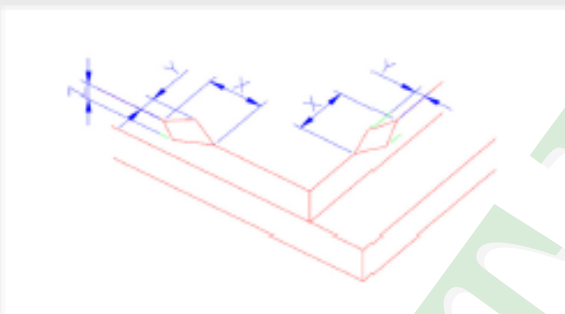
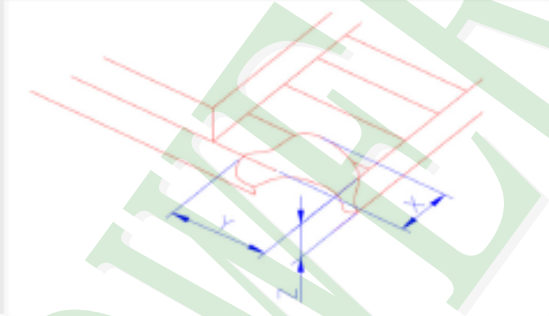

Zone D: IC Bonding Area

Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer.

### 3.2.1.5 Basic Principle

A set of sample to indicate the limit of acceptable quality level shall be discussed should a dispute occur.

### 3.2.1.6 Inspection Criteria

Number	Items	Criteria (mm)		
1.0 LCD Crack/ Broken	(1) The edge of LCD broken			
		X	Y	Z
Note: X: Length Y: Width Z: Height L: Length of ITO T: Height of LCD	(2) LCD corner broken			
		X	Y	Z
	(3) LCD crack			



Number	Items	Criteria (mm)				
2.0	Spot defects  $\Phi = (X+Y) / 2$	① Light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.10$		Ignore		
		$0.10 < \Phi \leq 0.25$		4(distance $\geq 10$ mm)		
		$0.25 < \Phi \leq 0.35$		3		
		$\Phi > 0.4$		0		
		② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.1$		Ignore		
		$0.10 < \Phi \leq 0.25$		4(distance $\geq 10$ mm)		
		$0.25 < \Phi \leq 0.35$		3		
		$\Phi > 0.40$		0		
		③ Polarizer accidented spot				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.2$		Ignore		
		$0.3 < \Phi \leq 0.5$		3(distance $\geq 10$ mm)		
		$\Phi > 0.5$		1		
		④ Pixel bad points (light dot, Dim dot, colour dot)				
		Size (mm)	Zone	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.15$		Ignore		
$0.2 < \Phi \leq 0.3$		2(distance $\geq 10$ mm)				
$\Phi > 0.4$		1				
⑤ Polarizer Bubble						
Size (mm)	Zone	Acceptable Qty				
		A	B	C		
$\Phi \leq 0.2$		Ignore				
$0.3 < \Phi \leq 0.4$		4(distance $\geq 10$ mm)				
$0.4 < \Phi \leq 0.5$		3				
$\Phi > 0.5$		1				

3.0	Line defect (LCD/TP/Polarizer black/white line, scratch, stain)	Width (mm)	Length (mm)	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.05$	Ignore	Ignore		
		$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 2$	Ignore	
		$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		
		$0.08 < W$	Define as spot defect			
4.0	SMT	Do not allow: missing parts, solderless connection, cold solder joint, miss match, the positive and negative polarity oppose				
5.0	Display colour & Brightness	1. Colour: Measuring the colour coordinates, The measurement standard according to the datasheet or samples 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples				
6.0	LCD Mura	By 5% ND filter invisible				

- Criteria (functional items)

Number	Items	Criteria
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed



## 5. PRECAUTION RELATING PRODUCT HANDLING

### 5.1 SAFETY

- 5.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

### 5.2 HANDLING

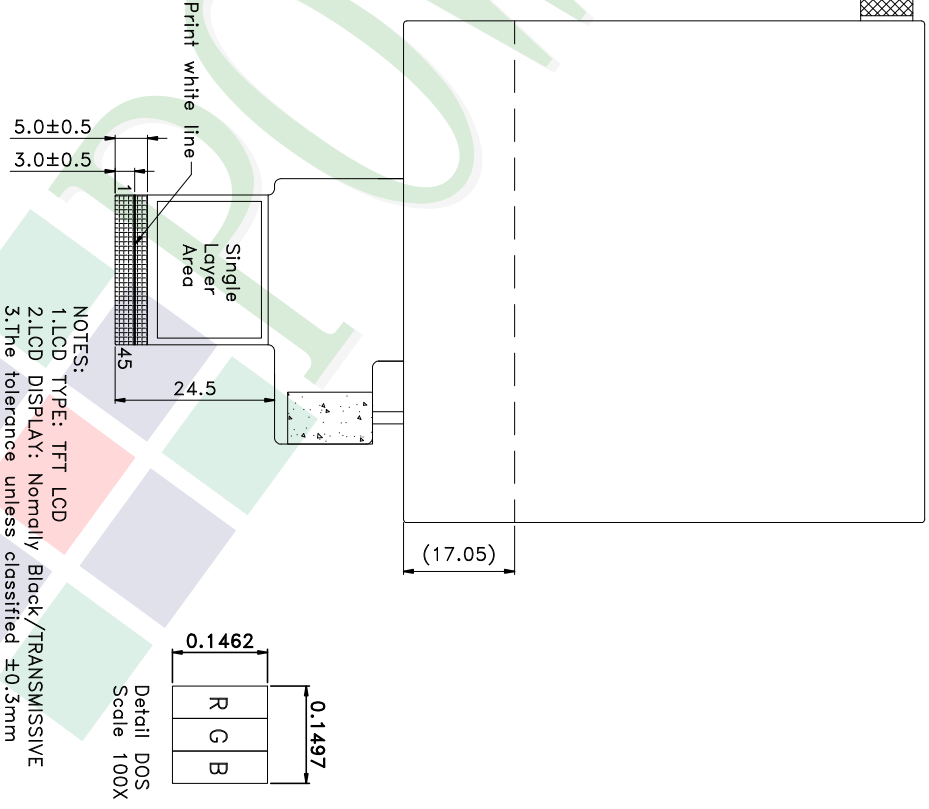
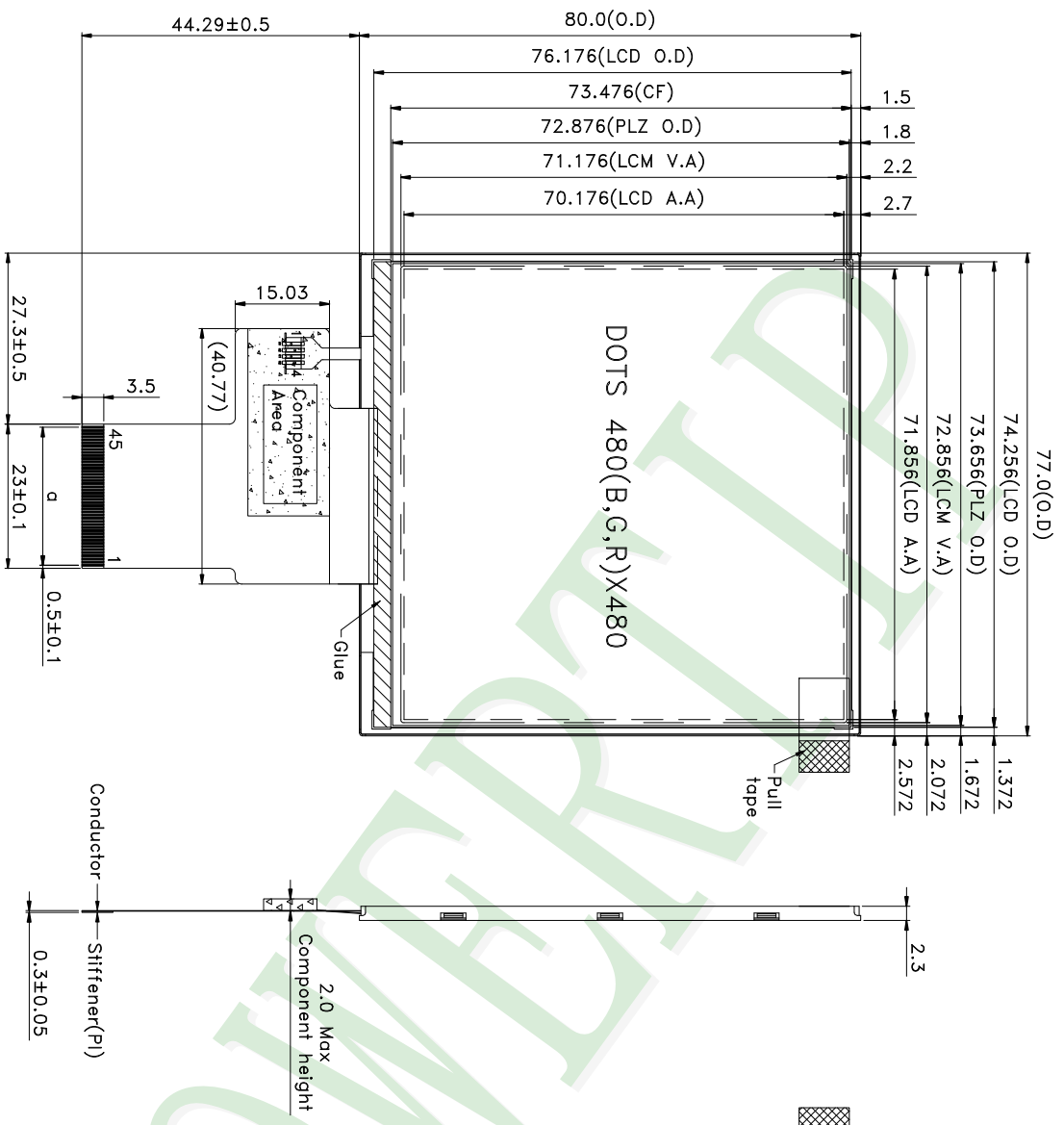
- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module, be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So, please handle it very carefully, do not touch, push or rub the exposed polarizing with anything harder than an HB pencil lead (glass, tweezers, etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands, this will stain the display area.
- 5.2.7 Do not use ketonic solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is  $320 \pm 10^{\circ}\text{C}$  and 3 ~ 5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM.
- 5.2.10 Caution! (LCM products with Capacitive Touch Panel)  
Strong EMI-sources such as switch-mode power supplies (SPS) can lead to touch malfunction (e.g., ghost-touches). Therefore, the touch needs to be thoroughly tested inside the target application.
- 5.2.11 CAUTION: Continuously displaying same static image will result in high possibility of image sticking/image burn-in effect due to TFT panel characteristic.
- 5.2.12 Double-sided tape designed to be attached with the customer's mechanical device, please follow up the rules and regulations published by the original manufacturer of double-side tape for the attachment operation.

### 5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$  and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush, shake, or jolt the module.

### 5.4 TERMS OF WARRANTY

- 5.4.1 Applicable warrant period  
The period is within thirteen months since the date of shipping out under normal using and storage conditions.
- 5.4.2 Unaccepted responsibility  
This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment, fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.



NOTES:  
 1. LCD TYPE: TFT LCD  
 2. LCD DISPLAY: Normally Black/TRANSMISSIVE  
 3. The tolerance unless classified  $\pm 0.5\text{mm}$   
 4.  $a=0.5X44=22.0\pm 0.1$ ;  $W=0.3\pm 0.05$   
 5. Kapton tape, Component Area(Unbending Area)  
 6. FPC suggested connector : FH12A-45S-0.55H(Hitrose) or compatible

007			
006			
005			
004			
003			
002			
001	NEW DRAWING	Clare	2023/12/15
REV	REV BY	REVISER	DATE

PART NO:		PH480480T001-ZHA	
DRAWING NAME:		LMD-PH480480T001-ZHA	
TITLE:		LCD MODULE DRAWING	

Design		Clare		Surface		Precision Level	
Check	Tina	Unit	MM	Material	1 ~ 4	1 ~ 4	-
Approve	Bright	Scale	FIT	Thickness	16 ~ 63	16 ~ 63	-
		Page	1/1	Quantity	63 ~ 250	250 ~ 1000	-

久正光電股份有限公司  
 POWER TIP TECHNOLOGY CORPORATION

Precision Level	
1 ~ 4	16 ~ 63
16 ~ 63	250 ~ 1000