TEXAS INSTRUMENTS

SN74LVC2G17

SCES381N – JANUARY 2002 – REVISED JANUARY 2015
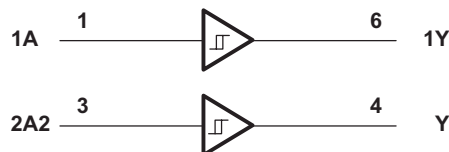
SN74LVC2G17 Dual Schmitt-Trigger Buffer

1 Features

- Schmitt-Trigger inputs provide hysteresis
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.4 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode Operation and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theater
- MP3 Players/Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD/Digital and High-Definition (HDTVs)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

This dual Schmitt-Trigger buffer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G17 device contains two buffers and performs the Boolean function Y = A. The device functions as two independent buffers, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information[1]

PART NUMBER	PACKAGE (PIN)	BODY SIZE
SN74LVC2G17	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm
	SON (6)	1.45 mm × 1.00 mm
	SON (6)	1.00 mm × 1.00 mm
	DSBGA (6)	1.41 mm × 0.91 mm

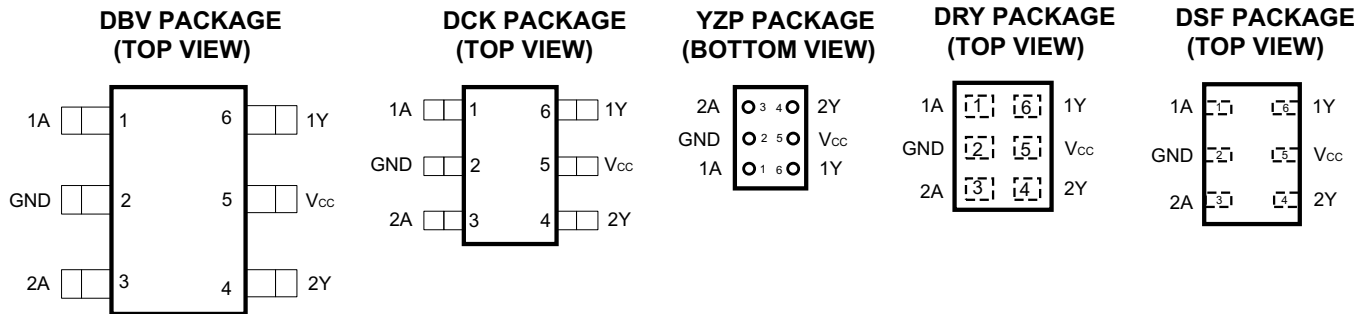(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

Table of Contents

5 Revision History

Changes from Revision M (November 2013) to Revision N   **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Changes from Revision L (September 2013) to Revision M   **Page**

- Updated document formatting. 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Condition*s table. 4

Changes from Revision K (July 2012) to Revision L   **Page**

- Updated document to new TI data sheet format. 1
- Added ESD warning. 12

Changes from Revision J (June 2012) to Revision K   **Page**

- Updated pin out graphic. 3

6 Pin Configuration and Functions

**DBV PACKAGE
(TOP VIEW)**

**DCK PACKAGE
(TOP VIEW)**

**YZP PACKAGE
(BOTTOM VIEW)**

**DRY PACKAGE
(TOP VIEW)**

**DSF PACKAGE
(TOP VIEW)**

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A	1	I	Input 1
1Y	6	O	Output 1
2A	3	I	Input 2
2Y	4	O	Output 2
GND	2	—	Ground
V$_{CC}$	5	—	Power Pin

Product Folder Links: *SN74LVC2G17*

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature under bias			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD} [1]	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]	2000	V
	Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins[3]	1000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Links: *SN74LVC2G17*

7.4 Thermal Information

THERMAL METRIC[1]	SN74LVC2G17					UNIT
	DBV	DCK	YZP	DRY	DSF	
	6 PINS					
$R_{\theta JA}$ Junction-to-ambient thermal resistance[2]	165	259	123	234	300	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	−40°C to 85°C			−40°C to 125°C			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{T+} Positive-going input threshold voltage			1.65 V	0.7		1.4	0.7		1.4	V
			2.3 V	1.0		1.7	1.0		1.7	
			3 V	1.3		2.0	1.3		2.0	
			4.5 V	1.9		3.1	1.9		3.1	
			5.5 V	2.2		3.7	2.2		3.7	
V_{T-} Negative-going input threshold voltage			1.65 V	0.3		0.7	0.3		0.7	V
			2.3 V	0.4		1	0.4		1.0	
			3 V	0.8		1.3	0.8		1.3	
			4.5 V	1.1		2	1.1		2.0	
			5.5 V	1.4		2.5	1.4		2.5	
ΔV_T Hysteresis $(V_{T+} - V_{T-})$			1.65 V	0.3		0.8	0.3		0.8	V
			2.3 V	0.4		0.9	0.35		0.9	
			3 V	0.4		1.1	0.4		1.1	
			4.5 V	0.6		1.3	0.6		1.3	
			5.5 V	0.7		1.4	0.7		1.4	
V_{OH}		$I_{OH} = -100$ µA	1.65 V to 5.5 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$			V
		$I_{OH} = -4$ mA	1.65 V	1.2			1.2			
		$I_{OH} = -8$ mA	2.3 V	1.9			1.9			
		$I_{OH} = -16$ mA	3 V	2.4			2.4			
		$I_{OH} = -24$ mA		2.3			2.3			
		$I_{OH} = -32$ mA	4.5 V	3.8			3.8			
V_{OL}		$I_{OL} = 100$ µA	1.65 V to 5.5 V			0.1			0.1	V
		$I_{OL} = 4$ mA	1.65 V			0.45			0.45	
		$I_{OL} = 8$ mA	2.3 V			0.3			0.3	
		$I_{OL} = 16$ mA	3 V			0.4			0.4	
		$I_{OL} = 24$ mA				0.55			0.55	
		$I_{OL} = 32$ mA	4.5 V			0.55			0.55	
I_I	A input	$V_I = 5.5$ V or GND	0 to 5.5 V			±5			±5	µA
I_{off}		V_I or $V_O = 5.5$ V	0			±10			±10	µA
I_{CC}		$V_I = 5.5$ V or GND, $I_O = 0$	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}		One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_i		$V_I = V_{CC}$ or GND	3.3 V		4			4		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25$°C.

7.6 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

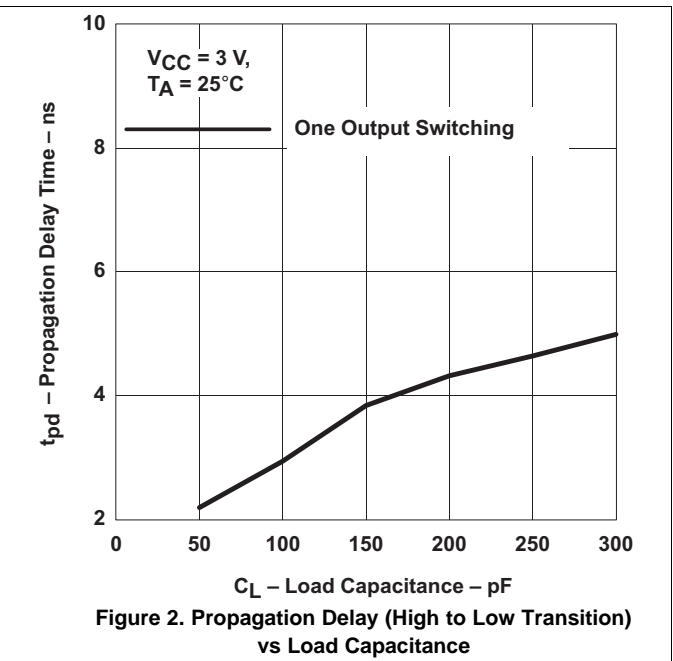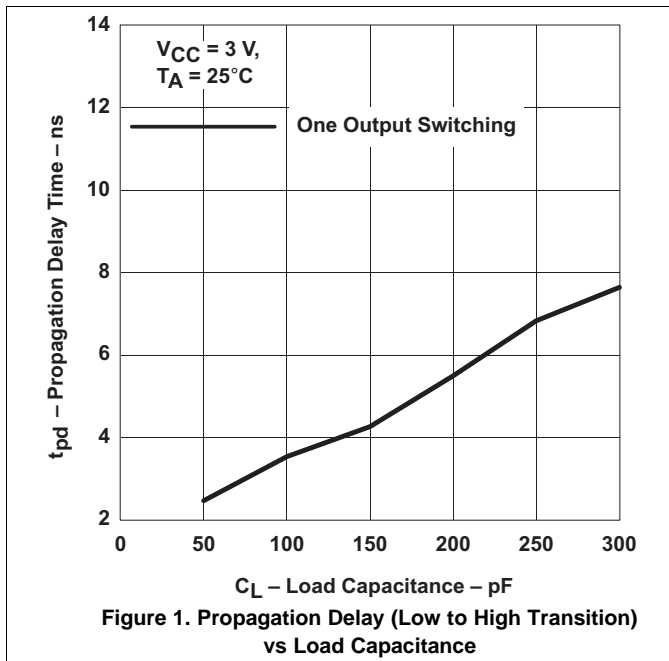| PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.9	9.3	1.9	5.7	2.2	5.4	1.5	4.3	ns

7.7 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.9	9.8	1.9	6.2	2.2	5.9	1.5	4.8	ns

7.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	17	18	19	21	pF

7.9 Typical Characteristics

Figure 1. Propagation Delay (Low to High Transition) vs Load Capacitance

Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance

Product Folder Links: *SN74LVC2G17*

8 Parameter Measurement Information

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V

**VOLTAGE WAVEFORMS
PULSE DURATION**
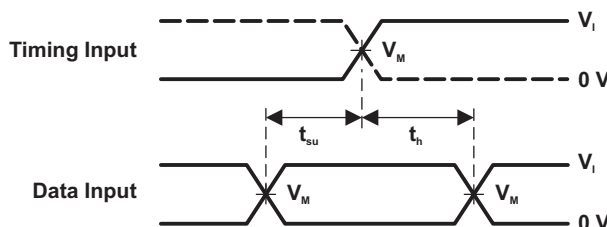
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74LVC2G17*

9 Detailed Description

9.1 Overview

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram
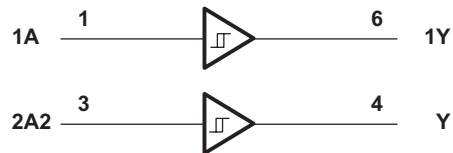
9.3 Feature Description

- 1.65 V to 5.5 V operating voltage range
- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8 V
- Inputs accept voltages to 5.5 V
  - 5-V tolerance on input pin
- I_{off} feature
  - Allows voltage on the inputs and outputs when V_{CC} is 0 V
  - Able to reduce leakage when V_{CC} is 0 V
- Schmitt-Trigger Input can improve the noise immunity capability

9.4 Device Functional Modes

INPUT A	OUTPUT Y
H	H
L	L

Product Folder Links: *SN74LVC2G17*

10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC2G17 device contains two buffers and performs the Boolean function Y = A. The device functions as two independent buffers, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

10.2 Typical Power Button Circuit
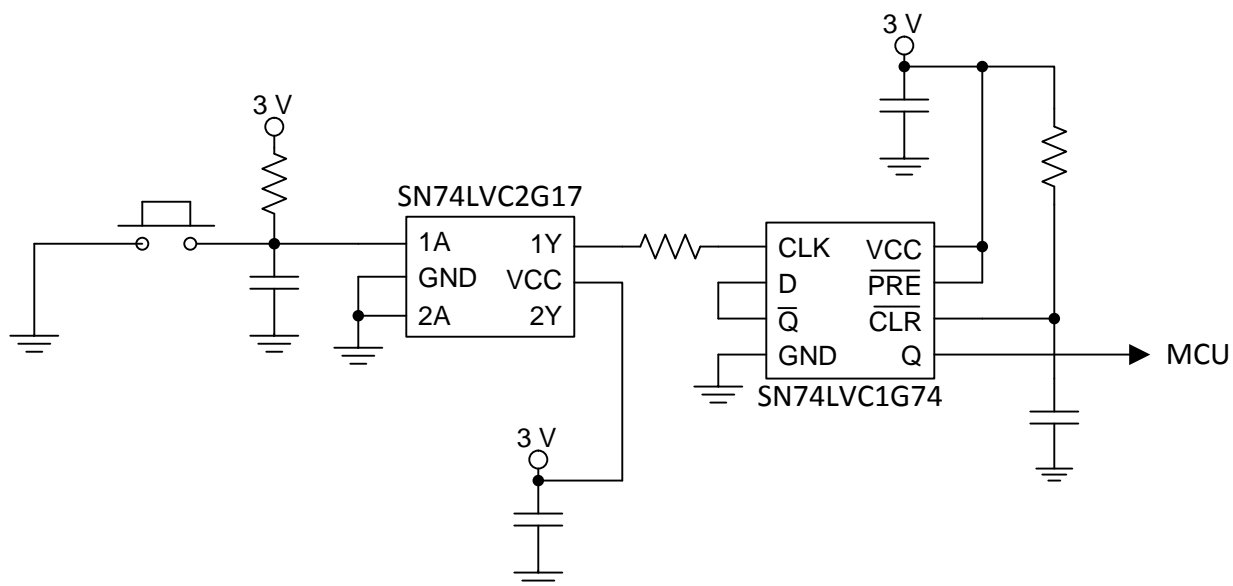
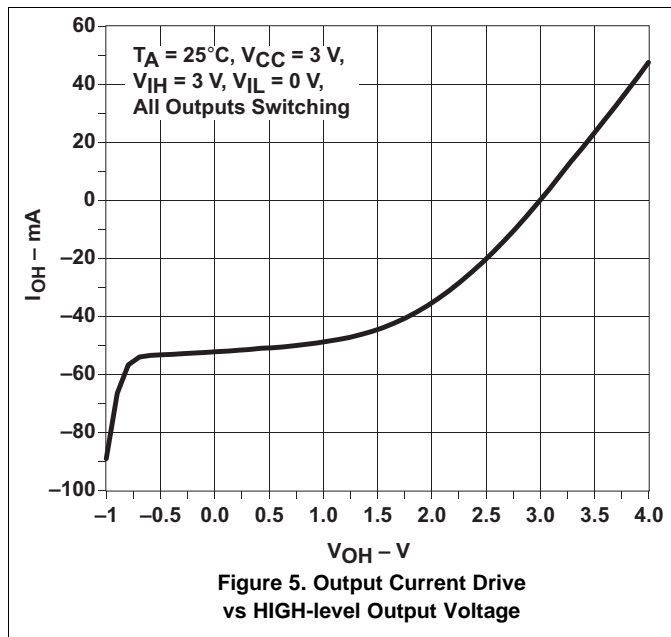**Figure 4. Device Power Button Circuit**

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see ($\Delta t/\Delta V$) in *Recommended Operating Conditions* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

Typical Power Button Circuit (continued)

10.2.3 Application Curves

$T_A = 25°C$, $V_{CC} = 3$ V, $V_{IH} = 3$ V, $V_{IL} = 0$ V, All Outputs Switching

Figure 5. Output Current Drive vs HIGH-level Output Voltage

$T_A = 25°C$, $V_{CC} = 3$ V, $V_{IH} = 3$ V, $V_{IL} = 0$ V, All Outputs Switching

Figure 6. Output Current Drive vs LOW-level Output Voltage
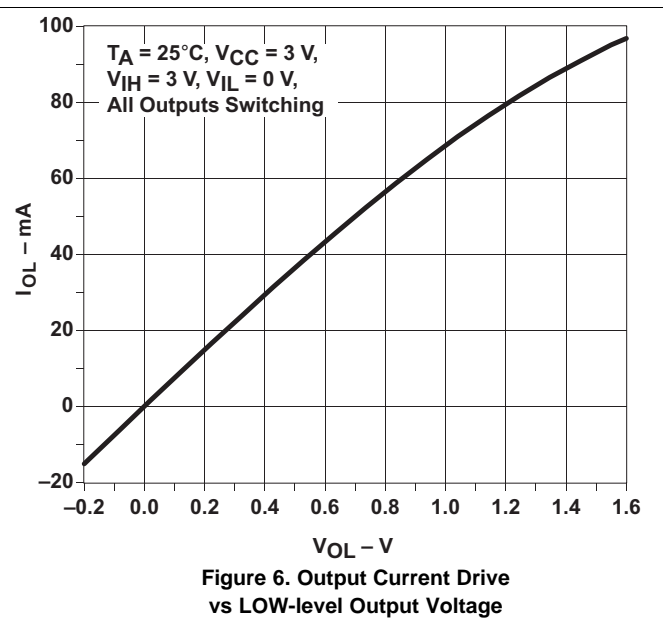
11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 µF or 0.022 µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.
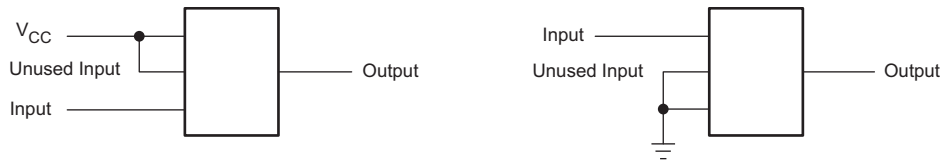
12.2 Layout Example

Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G17DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C175 ~ C17F ~ C17K ~ C17R)	Samples
SN74LVC2G17DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F	Samples
SN74LVC2G17DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C175 ~ C17F ~ C17K ~ C17R)	Samples
SN74LVC2G17DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F	Samples
SN74LVC2G17DCK3	ACTIVE	SC70	DCK	6	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 85	(C7F ~ C7Z)	Samples
SN74LVC2G17DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75 ~ C7F ~ C7K ~ C7R)	Samples
SN74LVC2G17DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75 ~ C7F ~ C7K ~ C7R)	Samples
SN74LVC2G17DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75 ~ C7F ~ C7K ~ C7R)	Samples
SN74LVC2G17DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75 ~ C7F ~ C7K ~ C7R)	Samples
SN74LVC2G17DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75 ~ C7F ~ C7K ~ C7R)	Samples
SN74LVC2G17DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75 ~ C7F ~ C7K ~ C7R)	Samples
SN74LVC2G17DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7	Samples
SN74LVC2G17DSF2	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7	Samples
SN74LVC2G17DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7	Samples
SN74LVC2G17YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(C77 ~ C7N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G17 :

● Automotive: SN74LVC2G17-Q1

● Enhanced Product: SN74LVC2G17-EP

NOTE: Qualified Version Definitions:

    ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G17DBVR	SOT-23	DBV	6	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC2G17DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC2G17DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2G17DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC2G17DBVT	SOT-23	DBV	6	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC2G17DBVTG4	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2G17DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC2G17DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC2G17DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2G17DCKT	SC70	DCK	6	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC2G17DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC2G17DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC2G17DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC2G17YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G17DBVR	SOT-23	DBV	6	3000	205.0	200.0	33.0
SN74LVC2G17DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2G17DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2G17DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC2G17DBVT	SOT-23	DBV	6	250	205.0	200.0	33.0
SN74LVC2G17DBVTG4	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC2G17DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC2G17DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC2G17DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC2G17DCKT	SC70	DCK	6	250	205.0	200.0	33.0
SN74LVC2G17DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC2G17DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC2G17DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC2G17YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0
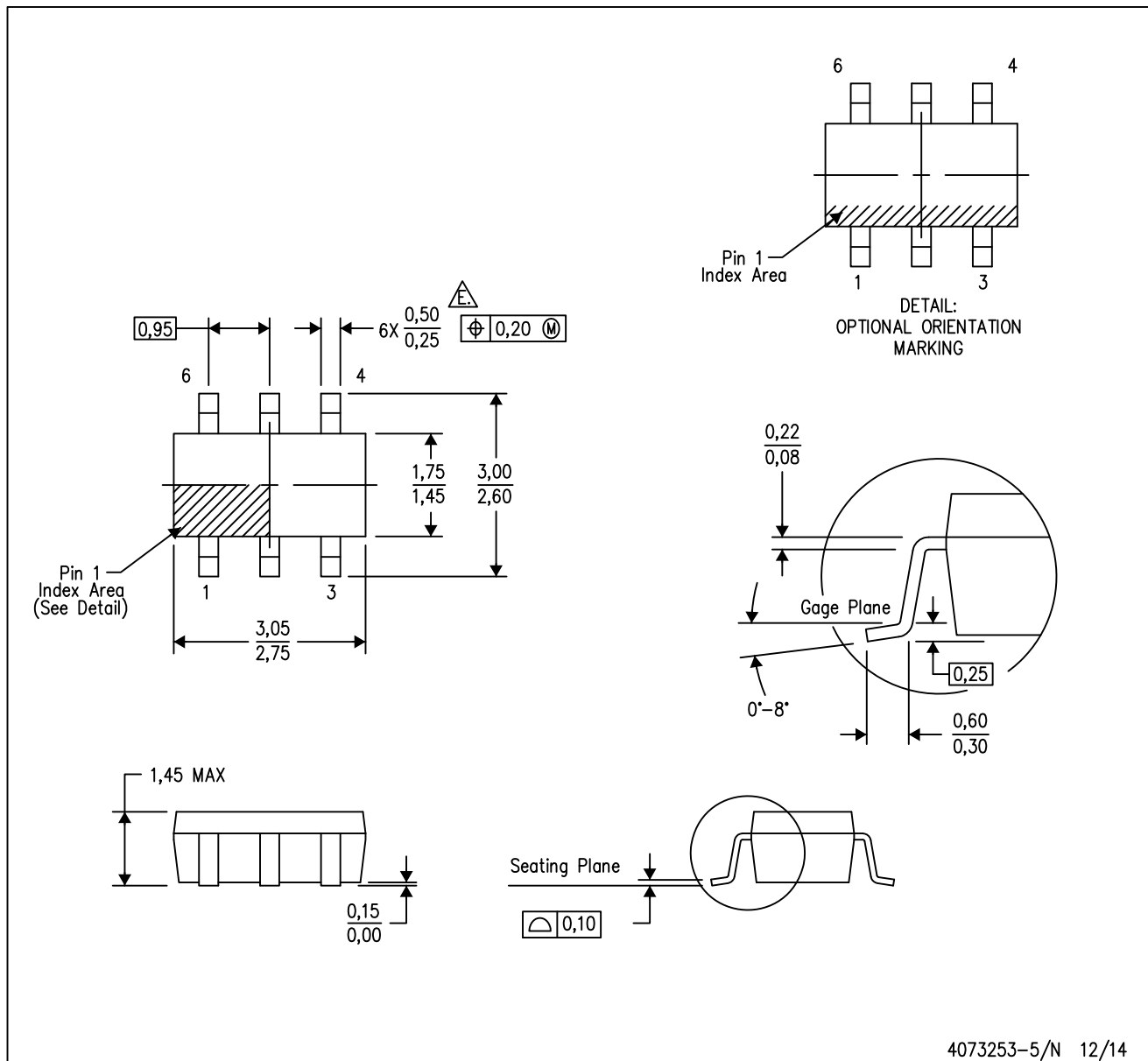
DBV (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE

DETAIL:
OPTIONAL ORIENTATION
MARKING

Pin 1
Index Area

4073253−5/N 12/14
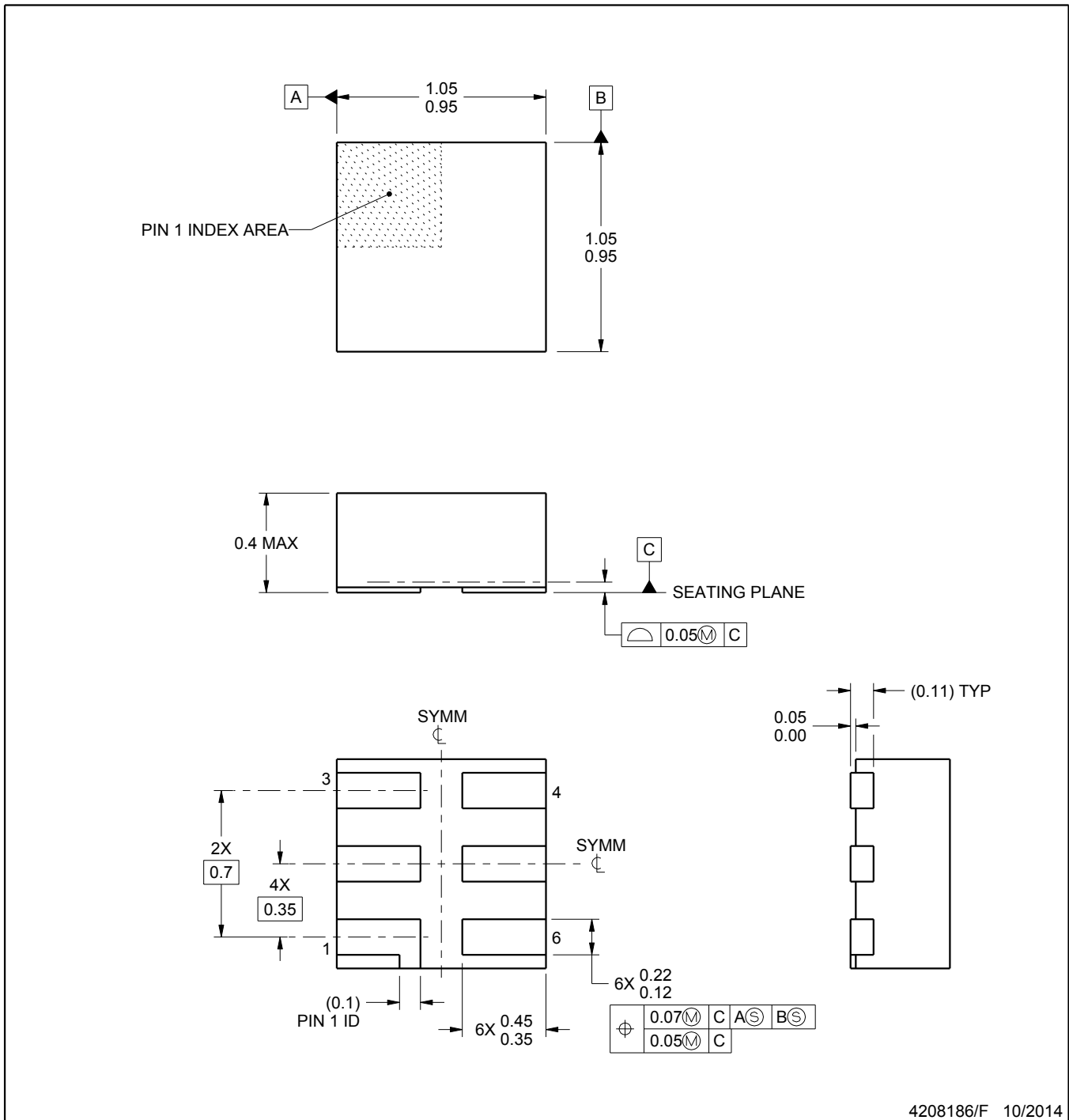
NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
         E. Falls within JEDEC MO−178 Variation AB, except minimum lead width.

DBV (R−PDSO−G6)   PLASTIC SMALL OUTLINE
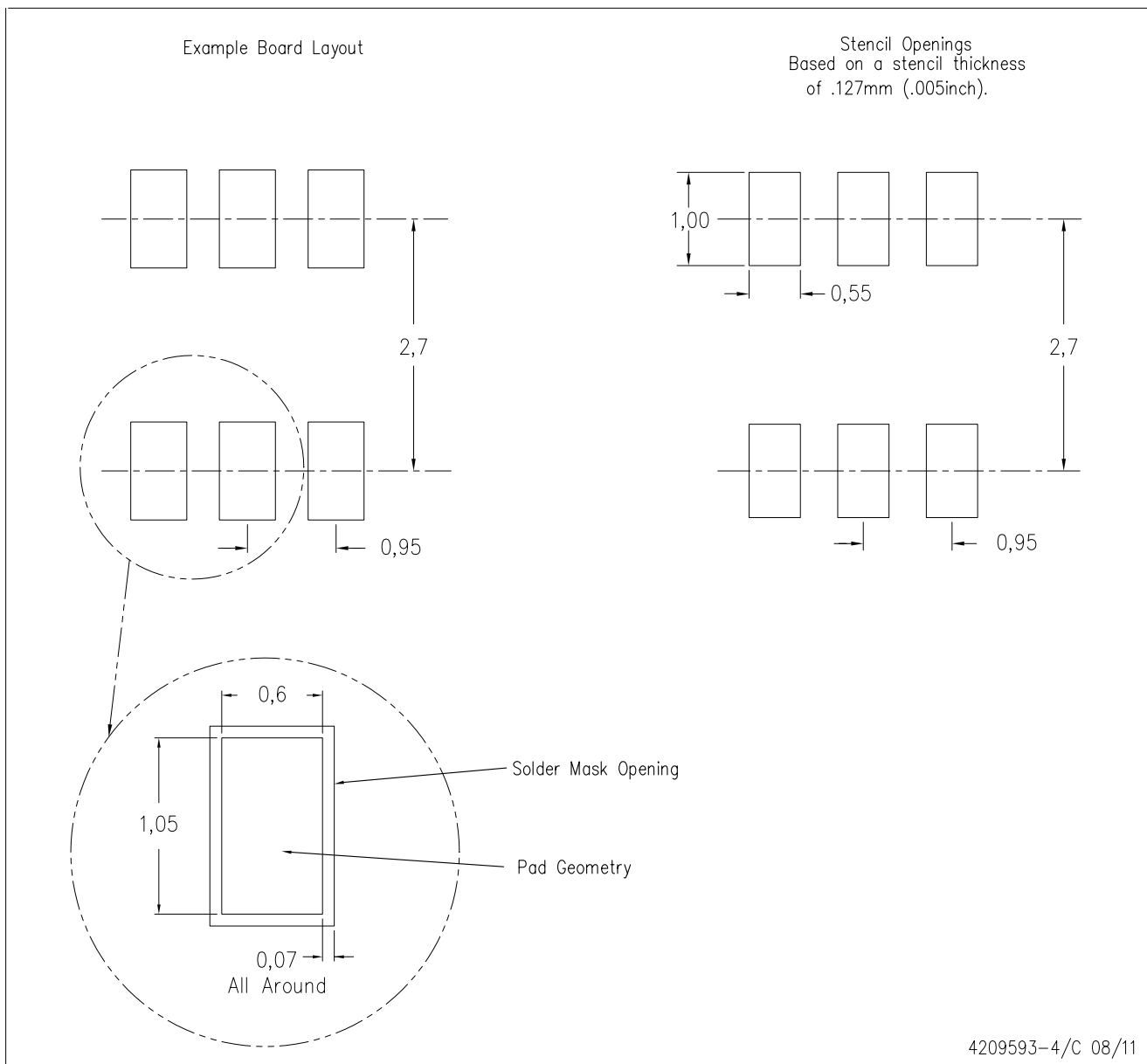
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−4/C 08/11

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D.   Publication IPC−7351 is recommended for alternate designs.
          E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
               metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

DCK (R−PDSO−G6) PLASTIC SMALL−OUTLINE PACKAGE

2,15 / 1,85

6   4

2,40 / 1,80

1,40 / 1,10

Pin 1
Index Area

1   3

0,65

6X 0,30 / 0,15

1,30

⊕ | 0,10 Ⓜ

0,22 / 0,08

Gauge Plane
Seating Plane

0,15

0°−8°

0,46 / 0,26

1,10 / 0,80

▱ | 0,10

Seating Plane

0,10 / 0,00

4093553−4/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
        D. Falls within JEDEC MO−203 variation AB.

DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

2x1,30

4x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

DRY (R−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

Pin 1 Index Area

$\dfrac{1,50}{1,40}$ [A]

[B]

$\dfrac{1,05}{0,95}$

$\dfrac{0,60}{0,51}$

// | 0,05 | C

0,15 Nominal
Lead Frame   [D]

Seating Plane

⌒ | 0,05 | C

[C]

$\dfrac{0,05}{0,00}$
Seating Height

1,00

0,50

6X $\dfrac{0,10}{0,00}$

5X $\dfrac{0,45}{0,25}$

[F] Pin 1 Identifier
Pin shape will be
modified per device.

5X $\dfrac{0,35}{0,25}$

6X $\dfrac{0,25}{0,15}$

⊕ | 0,10 Ⓜ | C | A | B
  | 0,05 Ⓜ | C

Bottom View
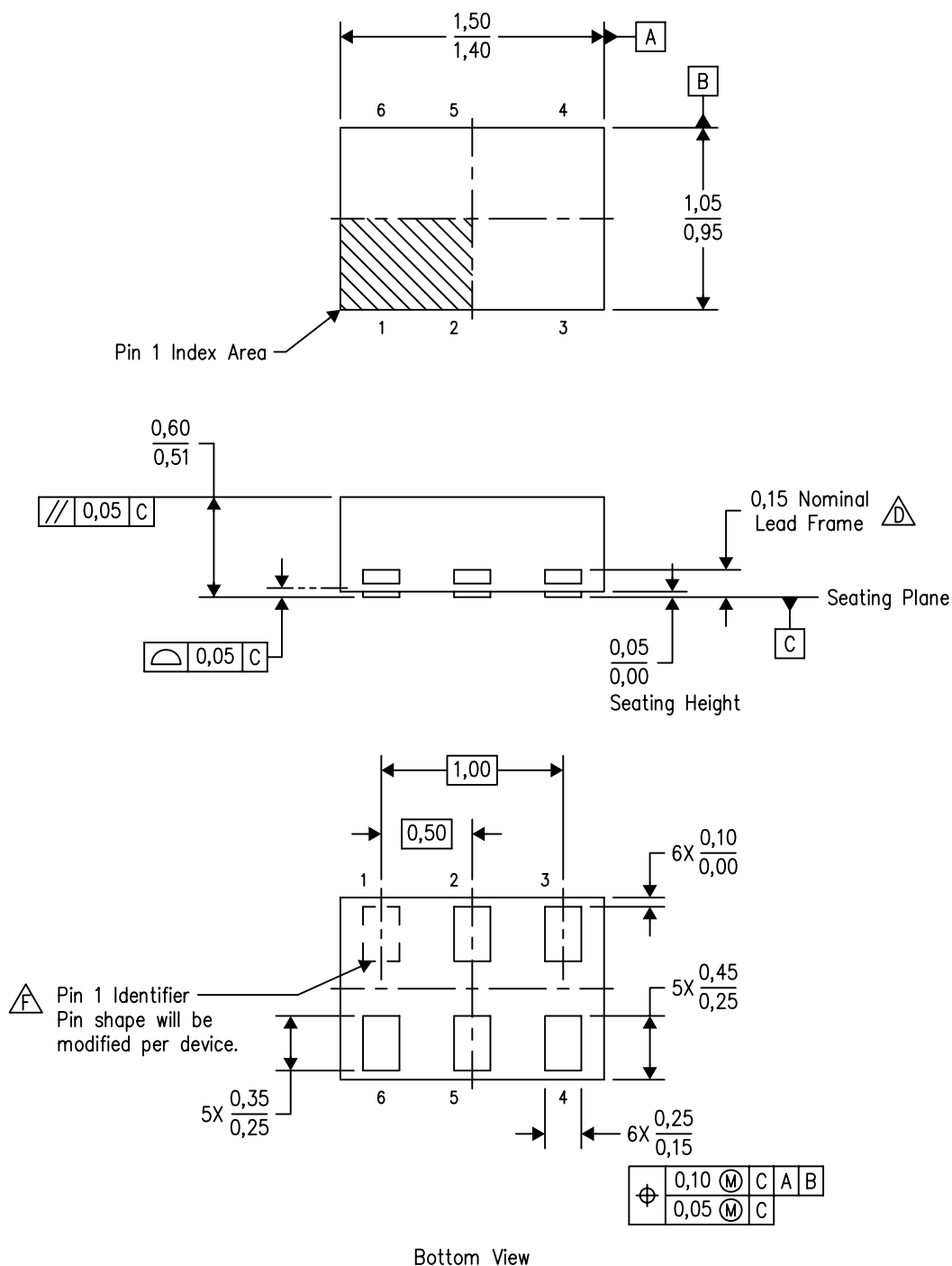
4207181/F   12/11

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
    B.   This drawing is subject to change without notice.
    C.   SON (Small Outline No−Lead) package configuration.
   [D]   The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
    E.   This package complies to JEDEC MO−287 variation UFAD.
   [F]   See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD
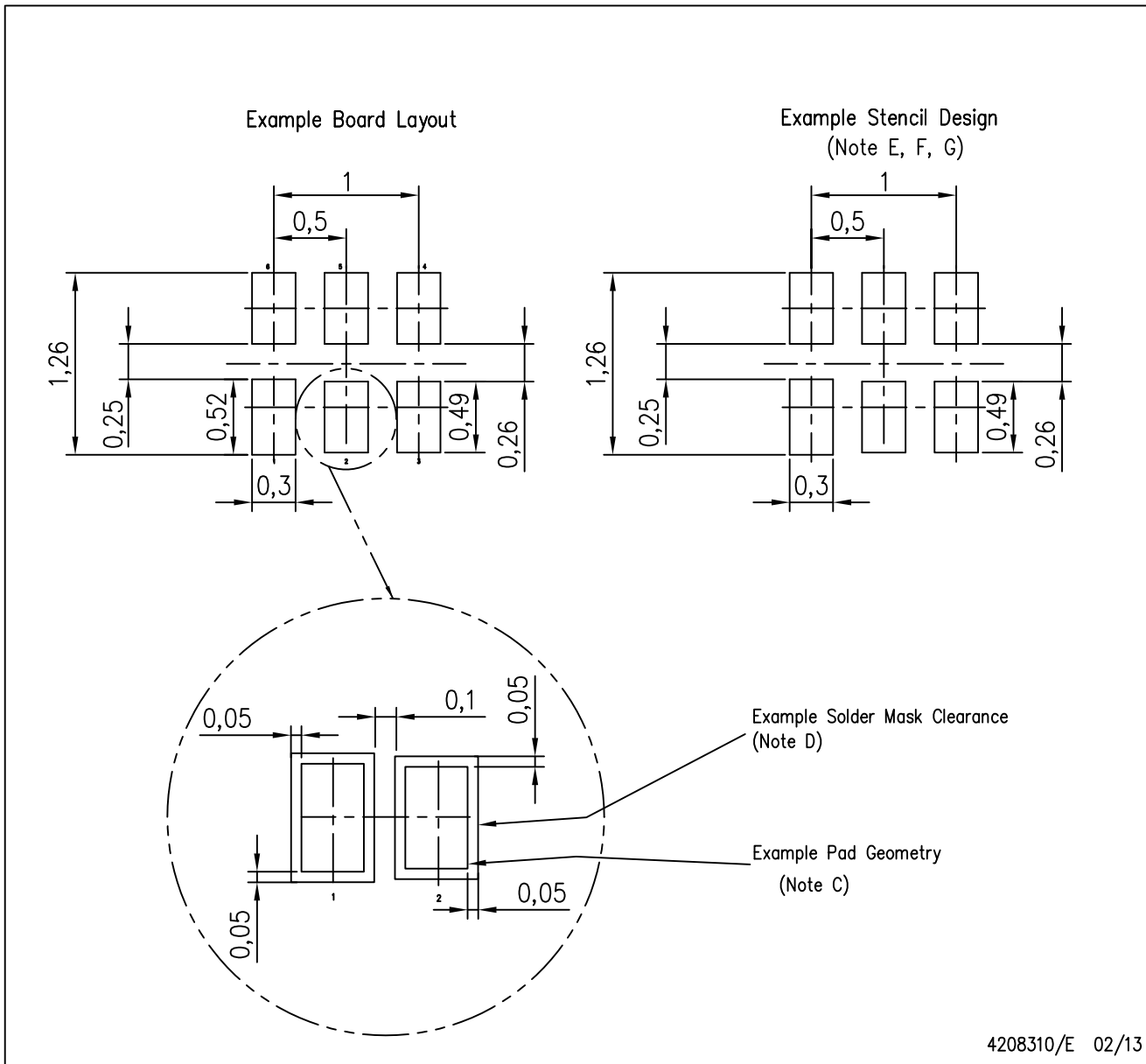
Example Board Layout

Example Stencil Design
(Note E, F, G)

4208310/E 02/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

Example Solder Mask Clearance
(Note D)

Example Pad Geometry
(Note C)

TEXAS INSTRUMENTS
www.ti.com

DSF (S-PX2SON-N6)   PLASTIC SMALL OUTLINE NO-LEAD

4208186/F   10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S–PX2SON–N6)   PLASTIC SMALL OUTLINE NO–LEAD

Land Pattern

0.20
0.35
0.53
0.15 1.20
0.70

Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

0.53
0.20

Stencil Pattern

0.165
0.35
0.53
0.15 1.20
0.70
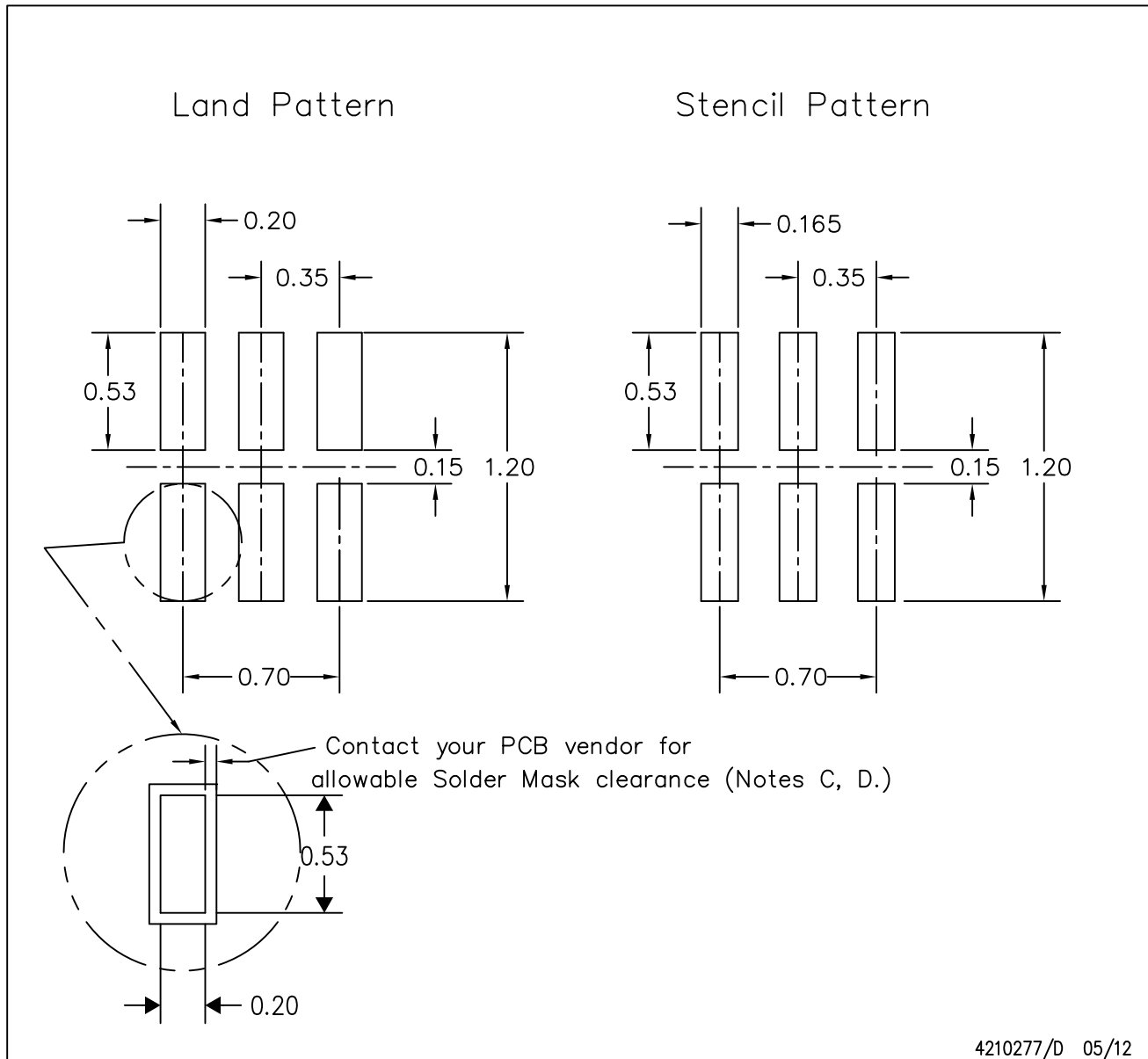
4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC–7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
            If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
        E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
        H. Component placement force should be minimized to prevent excessive paste block deformation.

TEXAS
INSTRUMENTS
www.ti.com

BALL A1
CORNER

B | E | A

D

0.5 MAX

0.19
0.15

BALL TYP

C

SEATING PLANE

⌒ | 0.05 | C

0.5 TYP

C

SYMM
⊄
B

A

1

2

SYMM
⊄

0.5
TYP

1
TYP
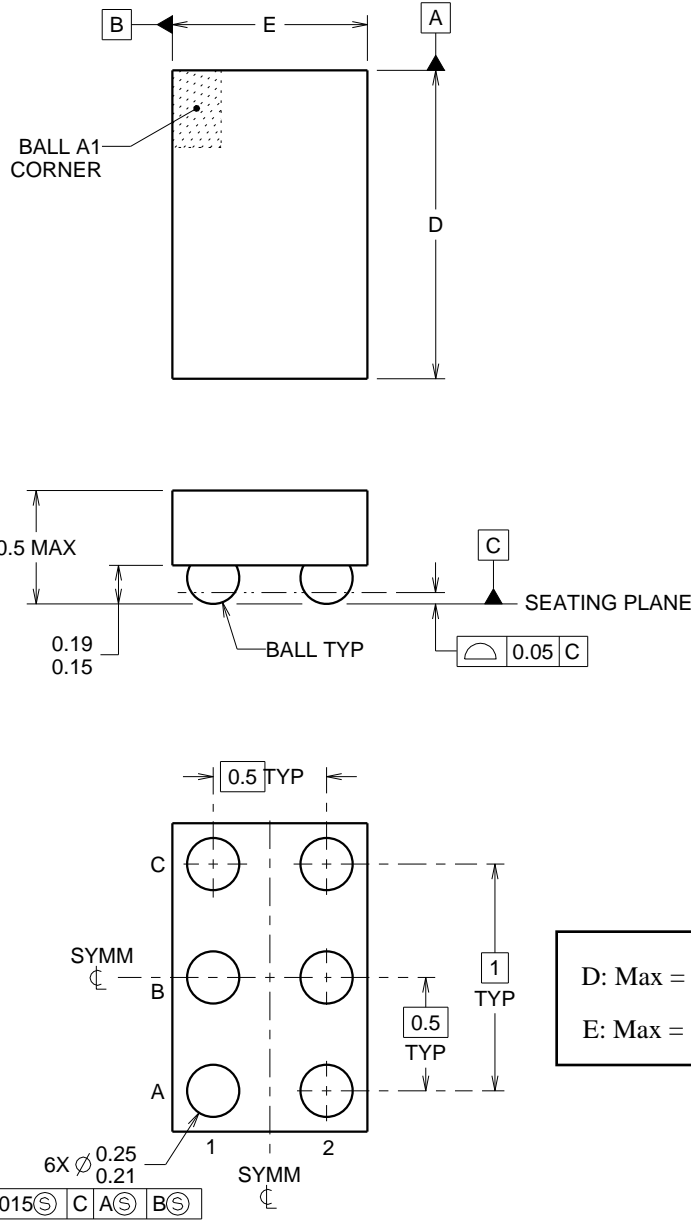
D: Max = 1.418 mm, Min =1.357 mm

E: Max = 0.918 mm, Min =0.857 mm

6X ∅ 0.25
0.21

⊕ | 0.015 Ⓢ | C | A Ⓢ | B Ⓢ

4219524/A   06/2014

NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

6X (∅ 0.225)

(0.5) TYP

(0.5) TYP

SYMM
℄

SYMM
℄

LAND PATTERN EXAMPLE
SCALE:40X

(∅ 0.225)
METAL

0.05 MAX

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

METAL
UNDER
MASK

(∅ 0.225)
SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219524/A   06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

(0.5) TYP

6X (☐0.25)

1

2

(R0.05) TYP

A

(0.5)
TYP

B

SYMM
℄

METAL
TYP

C

SYMM
℄

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A   06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE

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