

LCD TFT Datasheet

Rev.1.2 2015-08-05

ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally white	/
Size	3.5	Inch
Viewing Direction	12:00 (without image inversion)	O' Clock
Gray Scale Inversion Direction	6:00	O' Clock
LCM (W × H × D)	77.70 x 64.70 x 7.15	mm³
Active Area (W × H)	70.08 × 52.56	mm ²
Dot Pitch (W × H)	0.73 × 0.219	mm²
Number Of Dots	320 (RGB) × 240	/
Controller IC	SSD1963	1
Backlight Type	6 LEDs	/
Surface Luminance	540	cd/m²
Interface Type	Parallel 8/16b (i80 by default)	/
Color Depth	262k	1
Pixel Arrangement	RGB Vertical Stripe	/
Input Voltage	3.3	V
With/Without TSP	Without touch panel	/
Weight	59	g

Note 1: RoHS compliant

Note 2: LCM weight tolerance: ± 5%.

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REVISION RECORD

REVNO.	REVDATE	CONTENTS	REMARKS
1.0	2014-05-16	Initial Release	
1.1	2015-01-30	Update surface luminance, update LED livetime,	
		update response time	
1.2	2015-08-05	Add pin numbering in the mechanical drawing	

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1. MODULE CLASSIFICATION INFORMATION

RV	Т	3.5	А	320240		F	W	N	36
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.

1.	BRAND	RV – Riverdi
2.	PRODUCT TYPE	T – TFT Standard F – TFT Custom
3.	DISPLAY SIZE	3.5 - 3.5" 4.3 - 4.3" 5.7 - 5.7" 7.0 - 7.0"
4.	MODEL SERIAL NO.	A (A-Z)
5.	RESOLUTION	320240 – 320x240 px 480272 – 480x272 px 800480 – 800x480 px
6.	INTERFACE	T – TFT LCD, RGB L – TFT LCD, LVDS C – TFT + Controller
7.	FRAME	N – No Frame F – Mounting Frame
8.	BACKLIGHT TYPE	W – LED White
9.	TOUCH PANEL	N – No Touch Panel R – Resistive Touch Panel C – Capacitive Touch Panel
10.	VERSION	36 (00-99)

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DIN	20							
PIN	20							
1	GND							
2	VDD	AE.	-	93.50— 86.00—	-1			
3	BL_E	vs FRAME	77	7.70 (FRAME O	D)————————————————————————————————————		Ē	
4	D/C	s>		3.90 (TFT OUTLI	· · · · · · · · · · · · · · · · · · ·	vs FRAME	φ	
5	WR	Ē		2.08 (TFT OPEN)			0 0	
6	RD	0.40 1.70 3.12	7	70.78 (TFT VA)- 70.08 (TFT AA)-	(3.06)		64.5 P.O. (PCF)	3)0.45PCB vs TFT
7	D0							
8	D1	1 1 1 1 1 1	⊕ S _A				(Ø3.50
9	D2					L l I		Ø3.50
10	D3	00)- (10)- (320*RGB*240			15.92	
11	D4	-64.70 (FRAME OD)—63.90 (TFT OUTLINE) -55.50 (TFT OPEN)— -53.26 (TFT VA) -52.56 (TFT AA)		1			(n)	
12	D5	FRAI FT C TFT S (TF		¥			Downstite	
13	D6	70 (F 30 (T 33.26					86: Downside	
14	D7	-64. 63.9 -55					29.99	
15	D8					n.	29.9	
16	D9		(ф)	<u> </u>		"		
17	D10	<u>, , , , , , , , , , , , , , , , , , , </u>				급	115	
18	D11							
19	D12							
20	D13							
21	D14				DETAIL A			
22	D15				SCALE 60:1			
23	NC				0.219		INTERNAL BACKLIGHT CIRCUIT DIAG	RAM
24	NC				↓			
25	cs				R G B		A	— K
26	RESET							
27 D	ISP_ON	NOTES:						
28	NC		TFT, TRANSMISS	SIVE. NORM	IALLY WHITE			
29	NC	2. OPERATION VOLTAGE:	VDD=3.3V	_, · · · - · · · ·				
30	NC		12 O'CLOCK					
31	NC	4. IC CONTROLLER:	SSD1963				CUSTOMER APVL	DATE 2015-08-05
32	NC	5. OPERATING TEMP.: 6. STORAGE TEMP.:	-20°C ~ 70°C -30°C ~ 80°C				DRAWN SCALE	1:1 TITLE
33	BLGND		6-LED WHITE, BL	III T-IN INVI	=RTFR		DFTG CHK UNIT	RVT3.5A320240CFWN36
	BLGND	8. SURFACE LUMINANCE:	540 cd/m^2	/IE			ENGR CHK	mm
35	BLVDD	9. GENERAL TOLERANCE:		1.1 Add	ding Pin information	2015.08.05	APPROVAL	MODEL
	BLVDD	10. RoHS COMPLIANT			al case	2015.05.30	' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	DWG NO PAGE
					ESCRIPTION	DATE	- RIVECII our pixels behave	Rev.1.1
				INEV. D	LOURIFHUN	DATE	Out bixers per leve	1,0,1,1



3. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage For Logic	VDD	-0.3	4.6	V
Input Voltage For Logic	VIN	-0.3	VDD	V
Input Voltage For LED Inverter	BLVDD	-0.3	7.0	V
Operating Temperature	TOP	-20	70	°C
Storage Temperature	T _{ST}	-30	80	°C
Humidity	RH	-	90% (Max 60°C)	RH

4. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Supply Voltage For Module	VDD	3.0	3.3	3.6	V	
Input Voltage for LED Inverter	BLVDD	2.8	3.3	5.5	V	
Input Voltage 'H' level for BL_E pin	BL_E _H	1.5	-	5.5	V	
Input Voltage 'L' level for BL_E pin	BL_E _L	0	-	0.7		
Input Current (Exclude LED Backlight)	IDD	-	25	32	mA	VDD = 3.3V
LED Backlight Current	IDD _{backlight}		150	187	mA	BLVDD=3.3V
LED Backlight Current	IDD _{backlight}		95	119	mA	BLVDD=5V
Total Input Current (Include LED	IDD _{total}	-	175	219	mA	BLVDD=3.3V
Backlight 100%)						
Input Voltage ' H ' level	V _{IH}	0.7VDD	-	VDD	V	
Input Voltage ' L ' level	V _{IL}	0	-	0.2VDD	V	
LED Life Time	-	40000	50000	-	Hrs	Note 1

Note 1: The LED life time is defined as the module brightness decrease to 50% original brightness at Ta=25°C.

5. ELECTRO-OPTICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	REMARK	NOTE
Response T	ime	Tr+Tf	0.00	-	25	30	ms	Figure 1	4
Contrast R	atio	Cr	θ=0° Ø=0°	-	350	-		Figure 2	1
Luminance Un	iformity	δ WHITE	-	75	80	-	%	Figure 2	3
Surface Lumi	nance	Lv	10-25 C	-	540	-	cd/m²	Figure 2	2
			Ø = 90°	30	40	-	deg	Figure 3	
Minusian Angle	Viewing Angle Range		Ø = 270°	50	60	-	deg	Figure 3	
viewing Angle			Ø = 0°	50	60	-	deg	Figure 3	6
			Ø = 180°	50	60	-	deg	Figure 3	U
	Red	х		0.574	0.624	0.674			
	Reu	У		0.318	0.368	0.418			
	Green	х	θ=0°	0.300	0.350	0.400			
CIE (x, y)		У	Ø=0°	0.500	0.550	0.600	Fi	gure 2	5
Chromaticity	Blue	х	<i>₩</i> -0 Та=25°С	0.093	0.143	0.193	''	igui e z	J
		У	18-25 C	0.069	0.119	0.169			
	White	х		0.260	0.310	0.360			
		У		0.283	0.333	0.383			
NTSC	-	-	-	-	50	-		%	-

Note 1. Contrast Ratio(CR) is defined mathematically as below, for more information see Figure 1.



Contrast Ratio = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \, WHITE \, = \, \frac{Minimum \, Surface \, Luminance \, with \, all \, white \, pixels \, (P1, P2, P3, P4, P5)}{Maximum \, Surface \, Luminance \, with \, all \, white \, pixels \, (P1, P2, P3, P4, P5)}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see Figure 1. The test equipment is Autronic-Melchers's ConoScope series.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

Note 6. Viewing angle is the angle at which the contrast ratio is greater than 2. For TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see Figure 3.

Note 7. For viewing angle and response time testing, the testing data is based on Autronic-Melchers's ConoScope series. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, CIE the test data is based on TOPCON's BM-5 photo detector.

Note 8. For TFT module, gray scale reverse occurs in the direction of panel viewing angle.

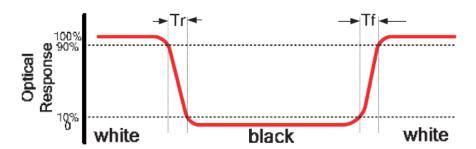


Figure 1. The definition of response time

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Figure 2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

A: 5 mm B: 5 mm H,V: Active Area

Light spot size \varnothing =5mm, 500mm distance from the LCD surface to detector lens

measurement instrument is TOPCON's luminance meter BM-5

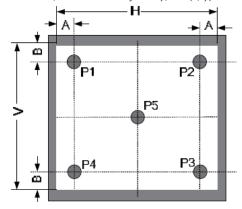
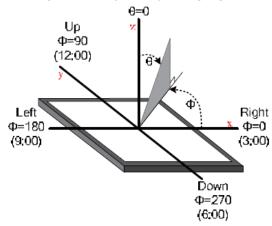


Figure 3. The definition of viewing angle



6. INTERFACE DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION					
1	GND	Р	Power Ground					
2	VDD	Р	Power Supply: +3.3V					
3	BL_E	ı	Backlight Control Signal, H: On/L: Off (internally pulled-up to BLVDD)					
4	D/C	ı	Data/Command Select					
5	WR	ı	Write Strobe Signal					
6	RD	ı	Read Strobe Signal					
7-22	D0-D15	ı	Data Bus. Pins not used should be floating.					
23	NC	-	No Connection					
24	NC	-	No Connection					
25	CS	I	Chip Select					
26	RESET	ı	Hardware reset					
27	DISP ON	I	Display Control H: On/L: Off (internally pulled-up)					
28	NC	-	No Connection					
29	NC	-	No Connection					
30	NC	-	No Connection					
31	NC	-	No Connection					
32	NC	-	No Connection					
33	BLGND	-	Backlight ground, can be connected to GND					
34	BLGND	-	Backlight ground, can be connected to GND					
35	BLVDD	-	Backlight power supply, can be connected to VDD					
36	BLVDD	-	Backlight power supply, can be connected to VDD					



7. INTERFACE TIMING CHARACTERISTICS

7.1. 8080 Mode

The 8080 mode MCU interface consist of CS#, D/C#, RD#, WR#, D[15:0]. This interface use WR# to define a write cycle and RD# for read cycle. If the WR# goes low when the CS# signal is low, the data or command will be latched into the system at the rising edge of WR#. Similarly, the read cycle will start when RD# goes low and end at the rising edge of RD#.

7.2. Pixel Data Format

Interface	Cycle	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
16 bits (565 format)	1 st			R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	В3	B2	B1
	1 st			R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
16 bits	2 nd			В7	В6	B5	В4	В3	B2	B1	В0	R7	R6	R5	R4	R3	R2	R1	R0
	3 rd			G7	G6	G5	G4	G3	G2	G1	G0	В7	В6	B5	В4	В3	B2	B1	В0
42.1.7	1 st							R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
12 bits	2 nd							G3	G2	G1	G0	В7	В6	B5	В4	В3	B2	B1	В0
0.1.11	1 st										R5	R4	R3	R2	R1	R0	G5	G4	G3
9 bits	2 nd										G2	G1	G0	B5	В4	В3	B2	B1	В0
	1 st											R7	R6	R5	R4	R3	R2	R1	R0
8 bits	2 nd											G7	G6	G5	G4	G3	G2	G1	G0
	3 rd											В7	В6	B5	В4	В3	B2	B1	В0

7.3. Parallel8080-series Interface Timing

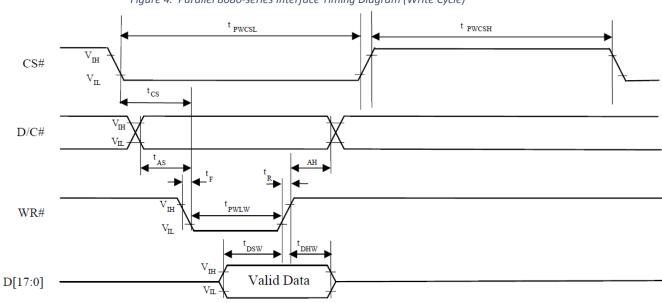
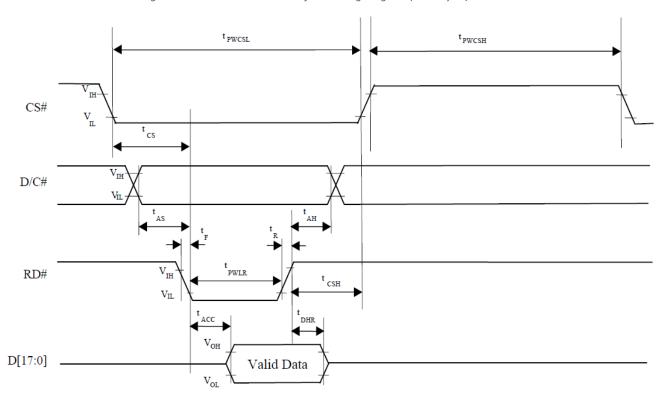


Figure 4. Parallel 8080-series Interface Timing Diagram (Write Cycle)



Figure 5.Parallel 8080-series Interface Timing Diagram (Read Cycle)



8. LCD TIMIG CHARACTERISTICS

8.1. Timing Chart

Timing parameter (VDD=3.3V, GND=0V, Ta=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK Clock Time	T _{clk}	1/Max(Fclk)	-	1/Min(F _{CLK})	ns	-
CLK Pulse Duty	T _{chw}	40	50	60	%	T _{CLK}
HSYNC to CLK	T _{hc}	-	-	1	CLK	-
HSYNC Width	T _{hwh}	1	-	-	CLK	-
VSYNC Width	T _{vwh}	1	-	-	ns	-
HSYNC Period Time	T _h	60	63.56	67	ns	-
VSYNC Set-up Time	T _{vst}	12	-	-	ns	-
VSYNC Hold Time	T _{vhd}	12	-	-	ns	-
HSYNC Setup Time	T _{hst}	12	-	-	ns	-
HSYNC Hold Time	T _{hhd}	12	-	-	ns	-
Data Set-up Time	T _{dsu}	12	-	-	ns	D00~D23 to CLK
Data Hold Time	T _{dhd}	12	-	-	ns	D00~D23 to CLK
DEN Set-up Time	T _{esu}	12	-	-	ns	DEN to CLK



Figure 6. DE mode timing diagram

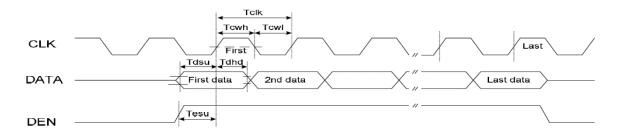


Figure 7. SYNC mode timing diagram

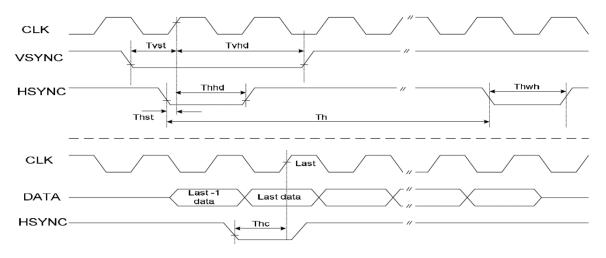
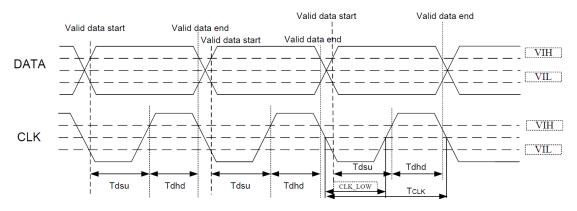


Figure 8. Timing diagram

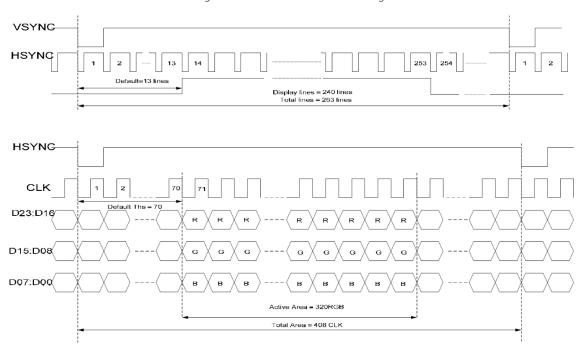




8.2. 24 Bit RGBMode for 320 x RGB x 240

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK Frequency	F _{clk}	7.0	8.0	9.0	MHz	VDD=3.0V~3.6V
CLK Cycle Time	T _{clk}	143	125	111	ns	-
CLK Pulse Duty	T _{cwh}	40	50	60	%	-
Time that HSYNC to	T _{hs}					DDLY=70
1st Data Input		40	70	255	CLK	Offset=0(fixed)
(NTSC)						

Figure 9. 24 bit RGB SYNC mode timing





9. RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	INSPECTION AFTER TEST			
1	High Temperature Storage	80±2°C/240 hours				
2	Low Temperature Storage	-30±2°C/240 hours				
3	High Temperature Operating	70±2°C/240 hours				
4	Low Temperature Operating	-20±2°C/240 hours				
5	Temperature Cycle	-30±2°C~25~70±2°C × 30 cycles				
6	Damp Proof Test	60°C ±5°C × 90%RH/160 hours				
7	Vibration Test	Frequency 10Hz~55Hz Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours For each direction of X, Y, Z (6 hours for total)	Inspection after 2~4 hours storage at room temperature, the sample shall be free from			
8	Mechanical Shock	60G 6ms, \pm X, \pm Y, \pm Z 3 times for each direction	defects: 1. Air bubble in the LCD			
9	Packing Drop Test	Height: 80 cm 1 corner, 3 edges, 6 surfaces	2. Seal leak3. Non-display			
10	Package Vibration Test	Random vibration: 0.015G ² /Hz from 5-200Hz -6dB/Octave from 200-500Hz 2 hours for each direction of X, Y, Z (6 hours for total)	 4. Missing segments 5. Glass crack 6. Current Idd is twice higher than initial value 7. The surface shall be free from damage 			
11	Electrostatic Discharge	Air: ± 8 KV 150 pF/ 330Ω 5 times Contact: ± 4 KV 150 pF/ 330Ω 5 times	8. Linearity must be no more than 1.5% by the linearity tester			
12	Hitting Test	1,000,000 times in the same point Hitting pad: tip R3.75mm, Silicone rubber, Hardness: 40deg. Load: 2.45N Hitting speed: Twice/sec Electric load: none Test area should be at 1.8mm inside of insulation.	9. The Electric characteristics requirements shall be satisfied			
13	Pen Sliding Durability Test	100,000 times minimum Hitting pad: tip R0.8mm plastic pen Load: 1.47N Sliding speed: 60 mm/sec Electric load: none Test area should be at 1.8mm inside of insulation.				

Remark:

- 1. The test samples should be applied to only one test item.
- 2. Sample size for each test item is 5~10pcs.
- 3. For Damp Proof Test, Pure water(Resistance
- 10M Ω) should be used.
- 4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
- 5. EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
- 6. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.



10.1 FGAL INFORMATION

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