

P33LF6QTKD

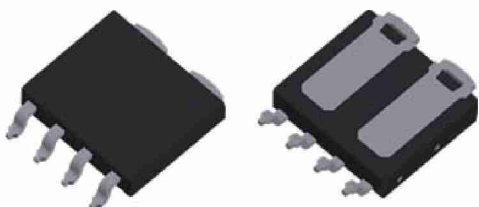
Power MOSFETs
60V, 33A, Dual N-channel

Feature

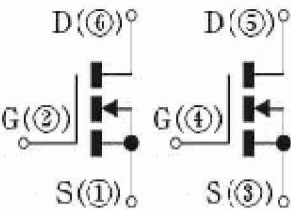
- N-channel
- Small SMD
- Dual type
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Halogen free
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): LF_Dual



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25°C, per FET)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel tempertature	Tch		-55 to 175	°C
Drain-source voltage	V _{DSS}		60	V
Gate-source voltage	V _{GSS}		±20	V
Continuous drain current(DC)	I _D		33	A
Continuous drain current(Peak)	I _{DP}	Pulse width 10μs, duty=1/100	99	A
Continuous source current(DC)	I _S		33	A
Total power dissipation	P _T	With heatsink	50	W
Total power dissipation	P _T	※	2.5	W
Total power dissipation	P _T	※	1.5	W
Single avalanche current	I _{AS}	Starting Tch=25°C Tch≤150°C	19	A
Single avalanche energy	E _{AS}	Starting Tch=25°C Tch≤150°C	40	mJ

※ :See the original Specifications

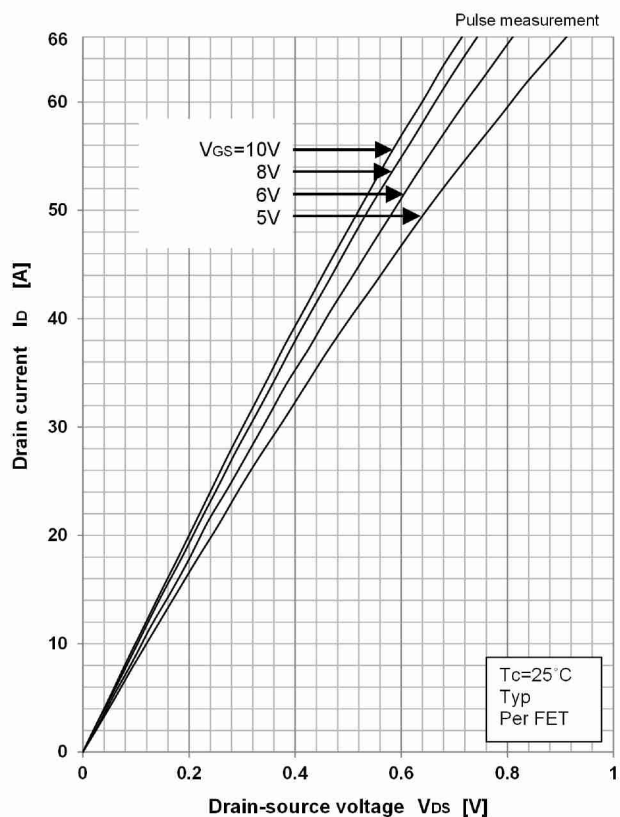
Electrical Characteristics (unless otherwise specified : Tc=25°C, per FET)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	60			V
Zero gate voltage drain current	I_{DSS}	VDS=60V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=16.5A, VDS=10V	7			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=16.5A, VGS=10V		0.01	0.0125	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=16.5A, VGS=4.5V		0.0131	0.0175	Ω
Gate threshold voltage	V_{th}	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=33A, VGS=0V			1.2	V
Thermal resistance	$R_{th(j-c)}$	Junction to case			2.98	°C/W
Thermal resistance	$R_{th(j-a)}$	Junction to ambient ※			60	°C/W
Thermal resistance	$R_{th(j-a)}$	Junction to ambient ※			100	°C/W
Total gate charge	Q_g	VDD=48V, VGS=10V, ID=33A		30		nC
Gate to source charge	Q_{gs}	VDD=48V, VGS=10V, ID=33A		7		nC
Gate to drain charge	Q_{gd}	VDD=48V, VGS=10V, ID=33A		9		nC
Input capacitance	C_{iss}	VDS=25V, VGS=0V, f=1MHz		1495		pF
Reverse transfer capacitance	C_{rss}	VDS=25V, VGS=0V, f=1MHz		84		pF
Output capacitance	C_{oss}	VDS=25V, VGS=0V, f=1MHz		181		pF
Turn-on delay time	$t_{d(on)}$	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		5		ns
Rise time	t_r	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		18		ns
Turn-off delay time	$t_{d(off)}$	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		18		ns
Fall time	t_f	ID=16.5A, RL=1.82Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4.5		ns
Diode reverse recovery time	t_{rr}	IF=33A, VGS=0V, di/dt=100A/μs		38		ns
Diode reverse recovery charge	Q_{rr}	IF=33A, VGS=0V, di/dt=100A/μs		37		nC

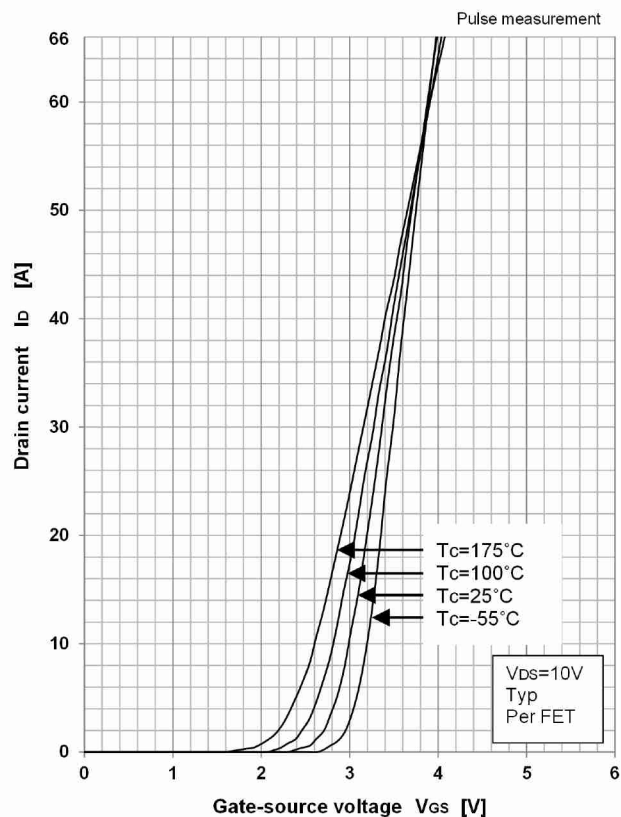
※ :See the original Specifications

CHARACTERISTIC DIAGRAMS

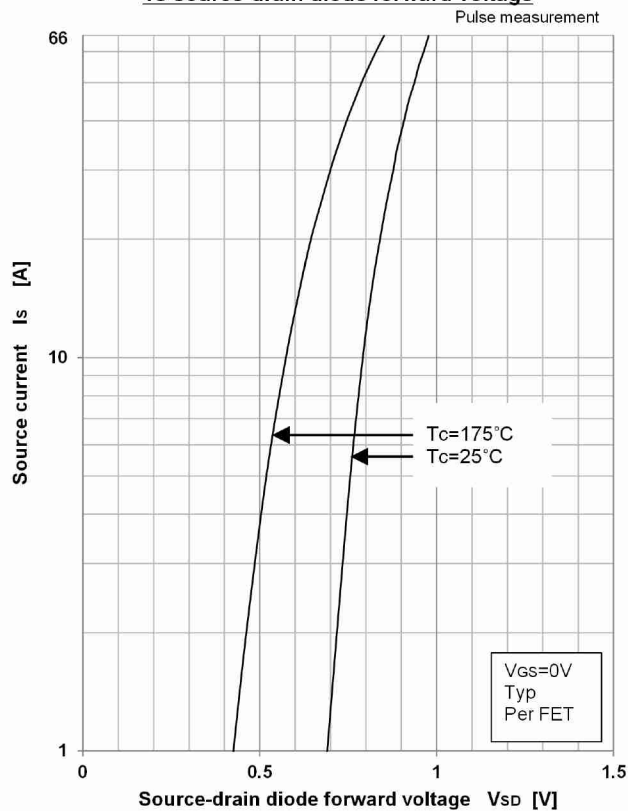
Typical output characteristics



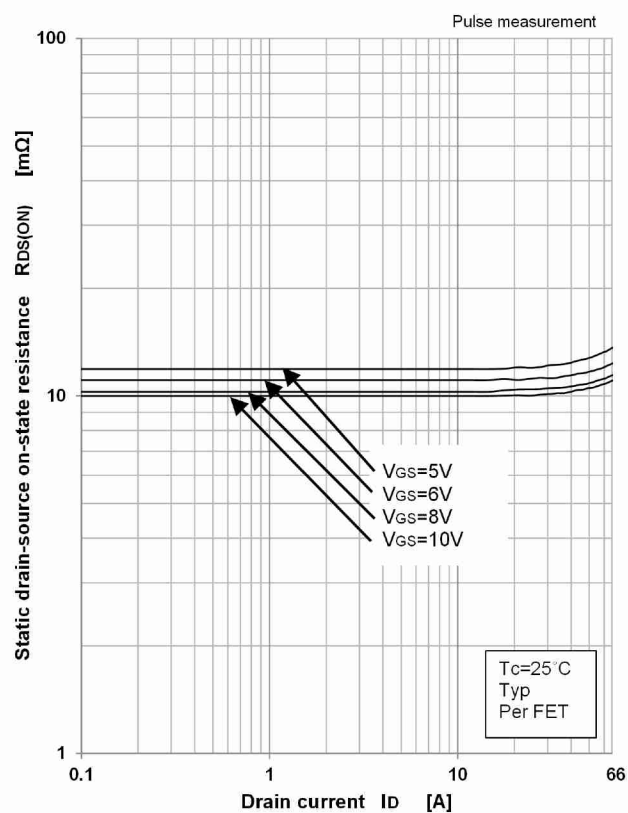
Transfer characteristics

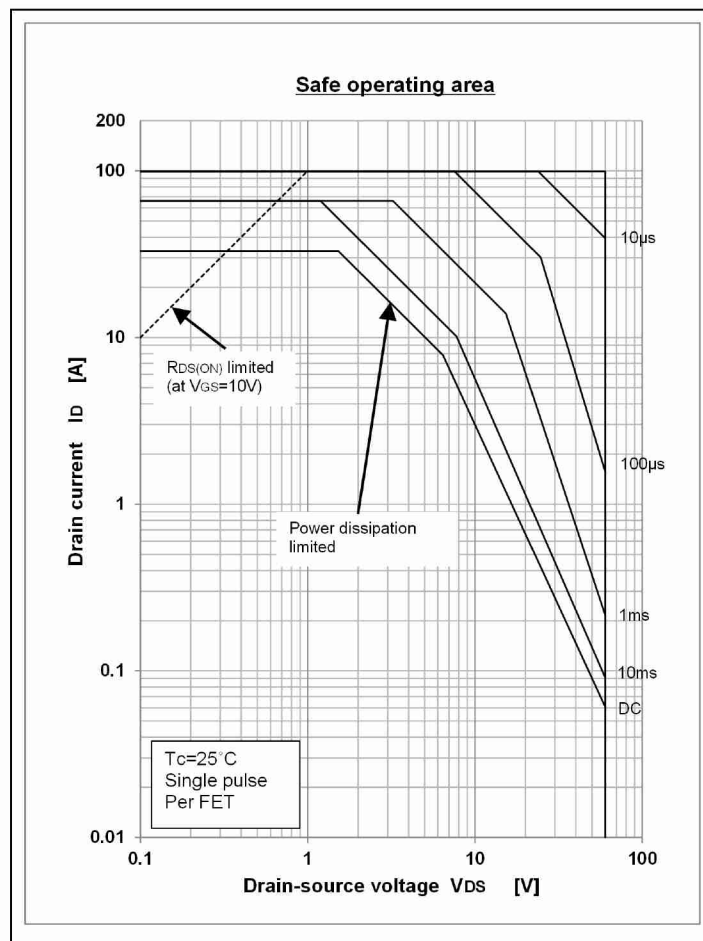
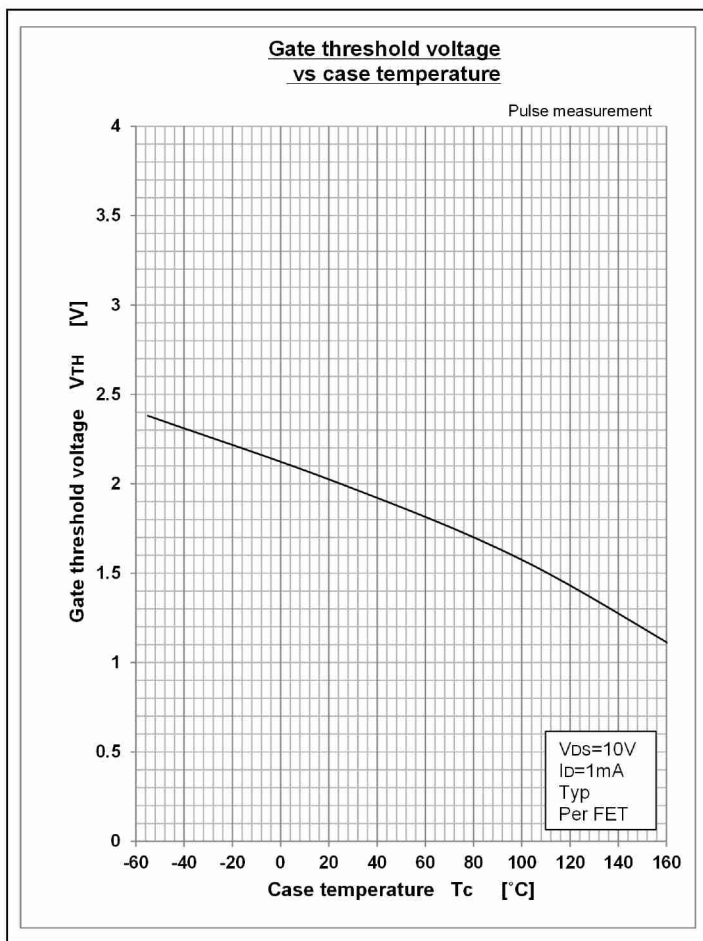
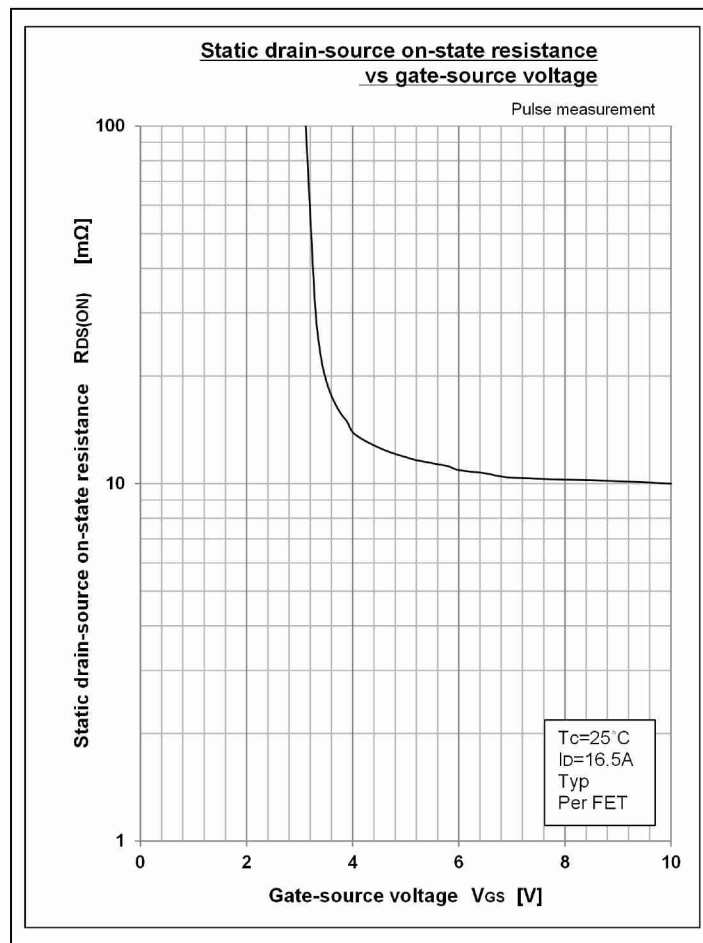
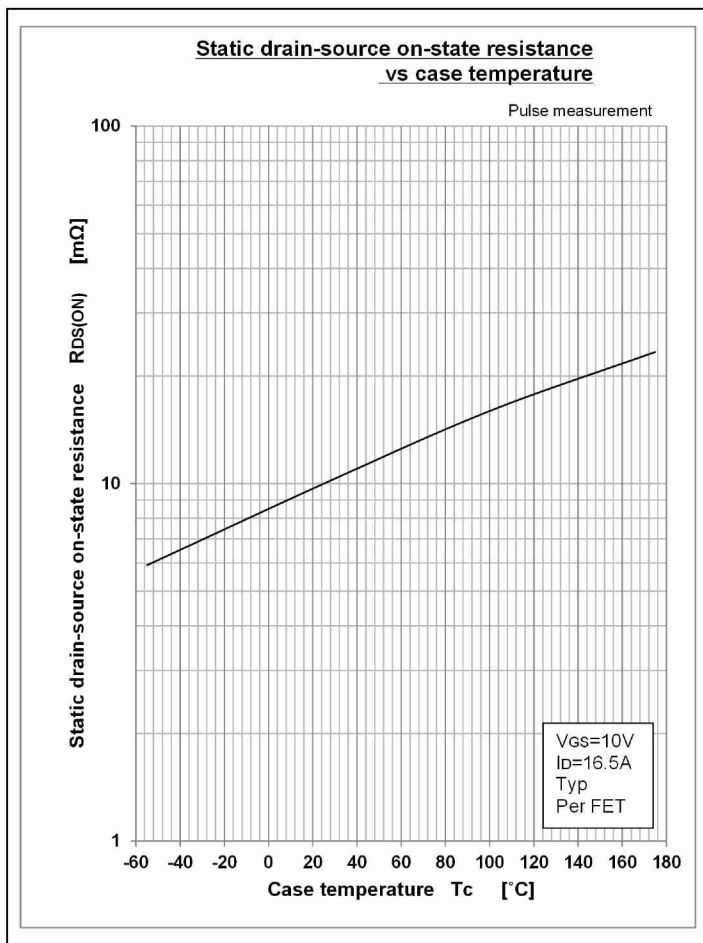


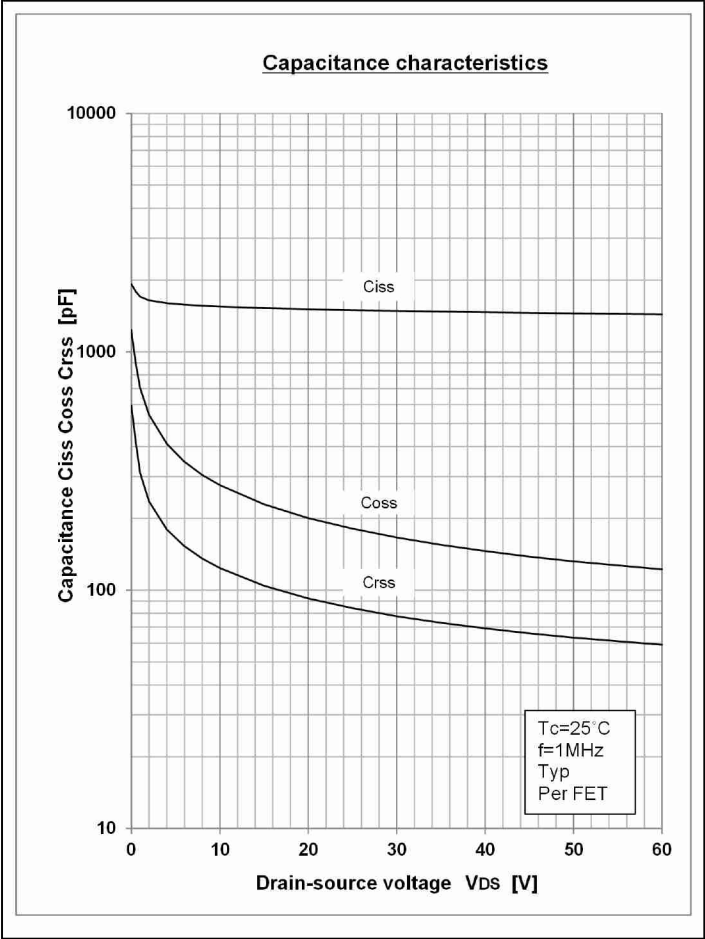
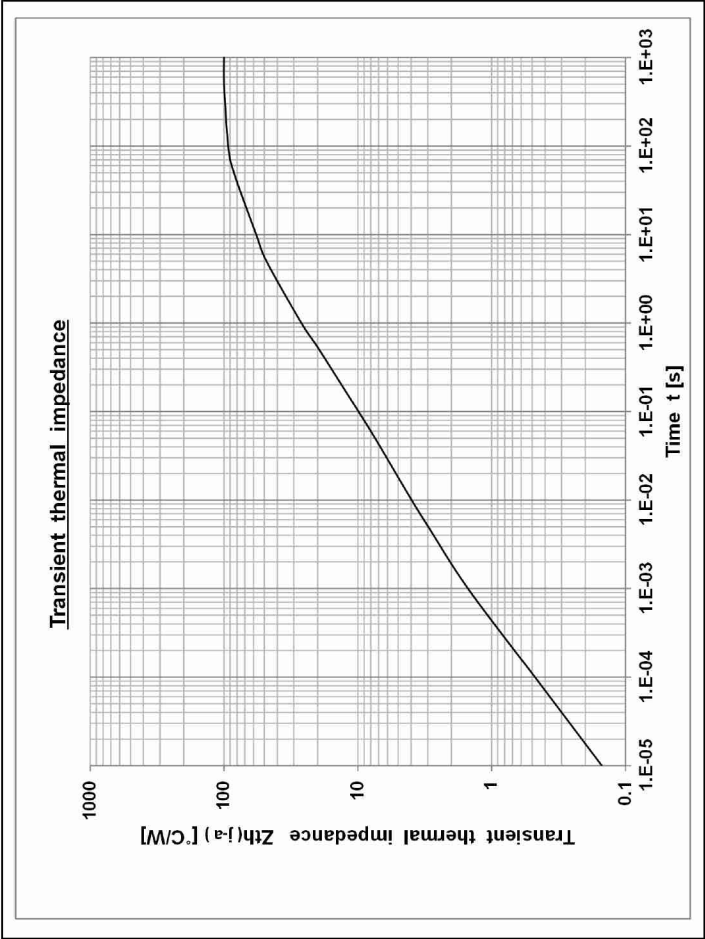
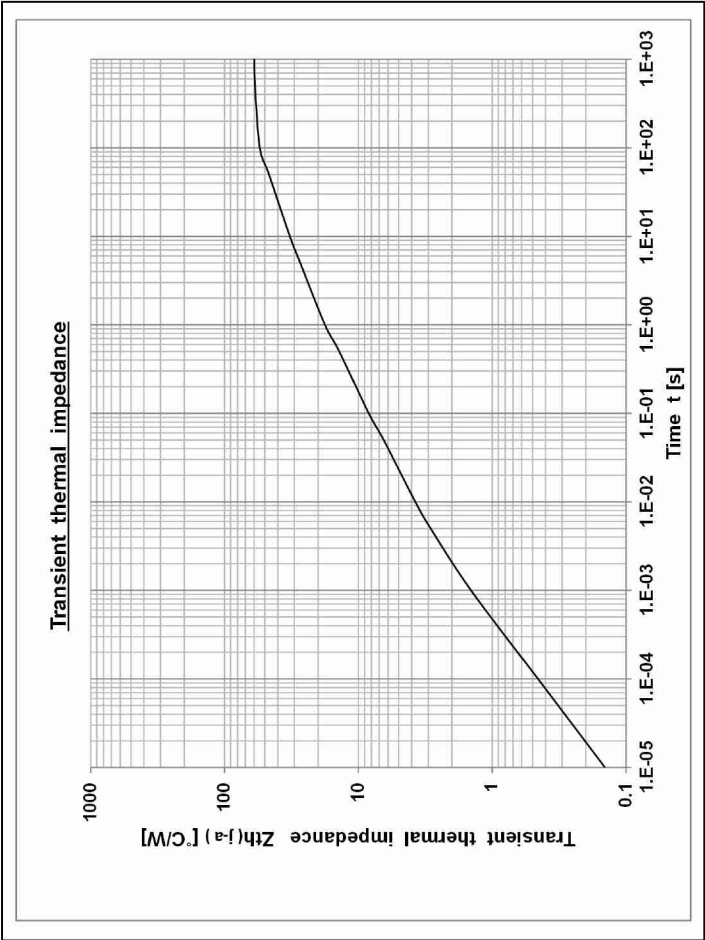
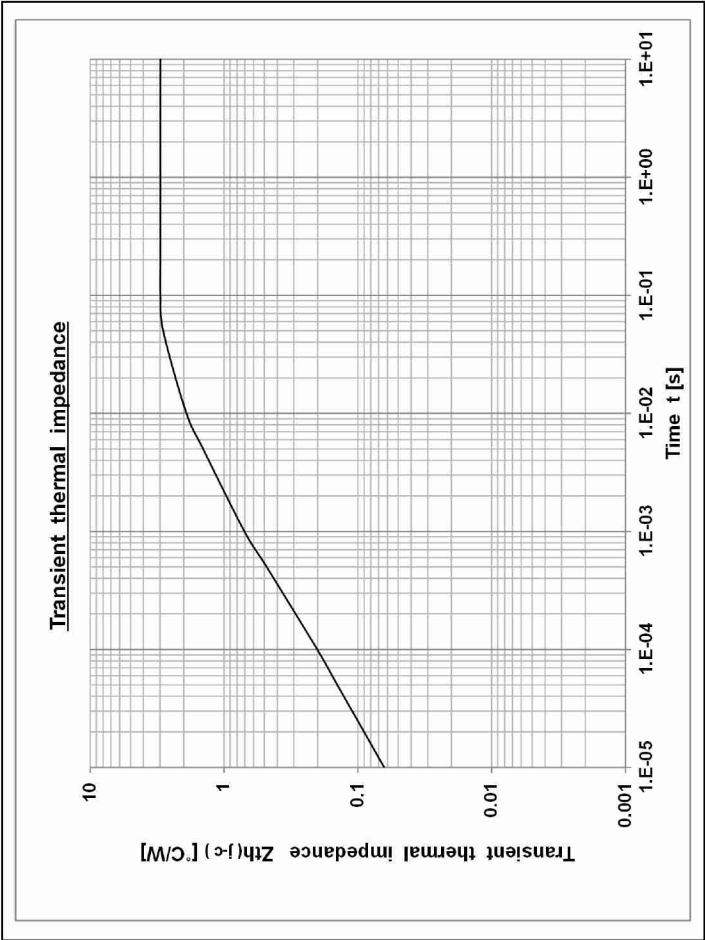
Source current vs source-drain diode forward voltage



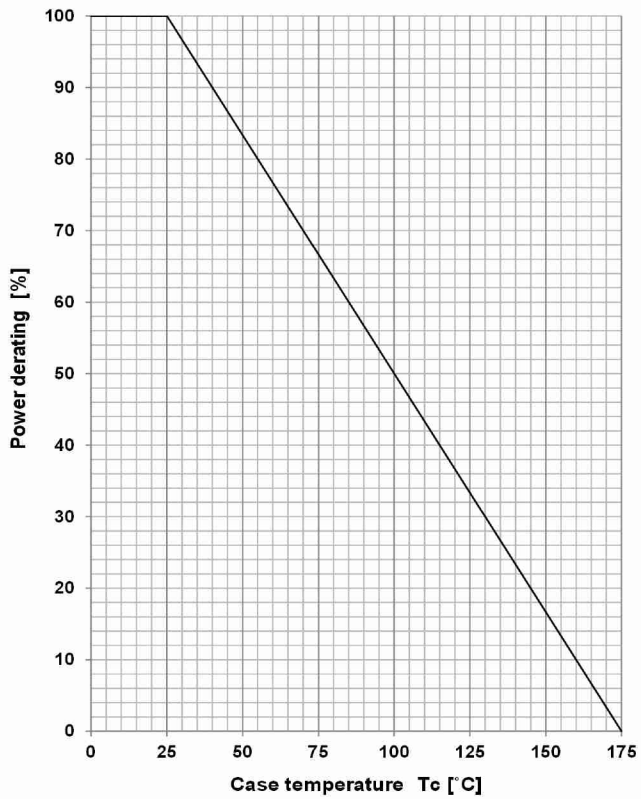
Static drain-source on-state resistance vs drain current



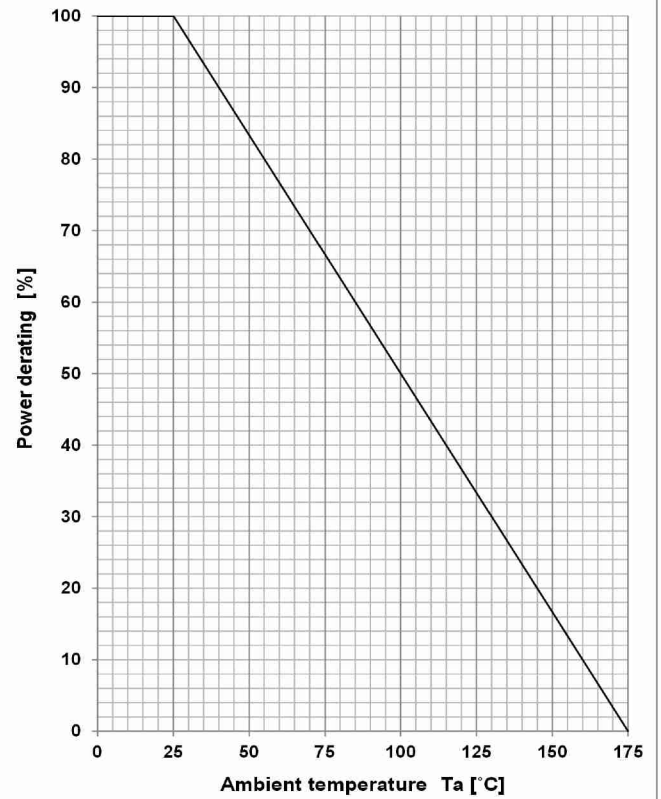




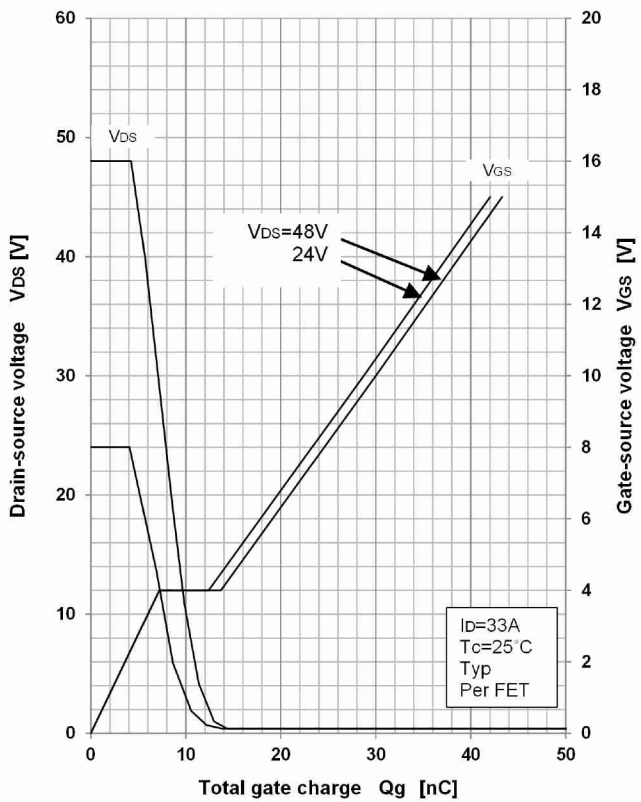
Power derating vs case temperature



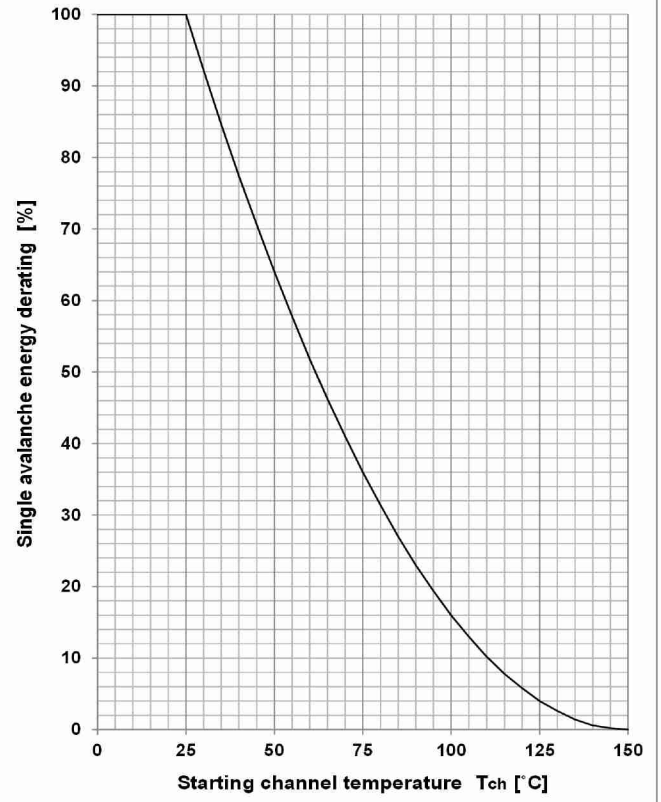
Power derating vs ambient temperature



Gate charge characteristics

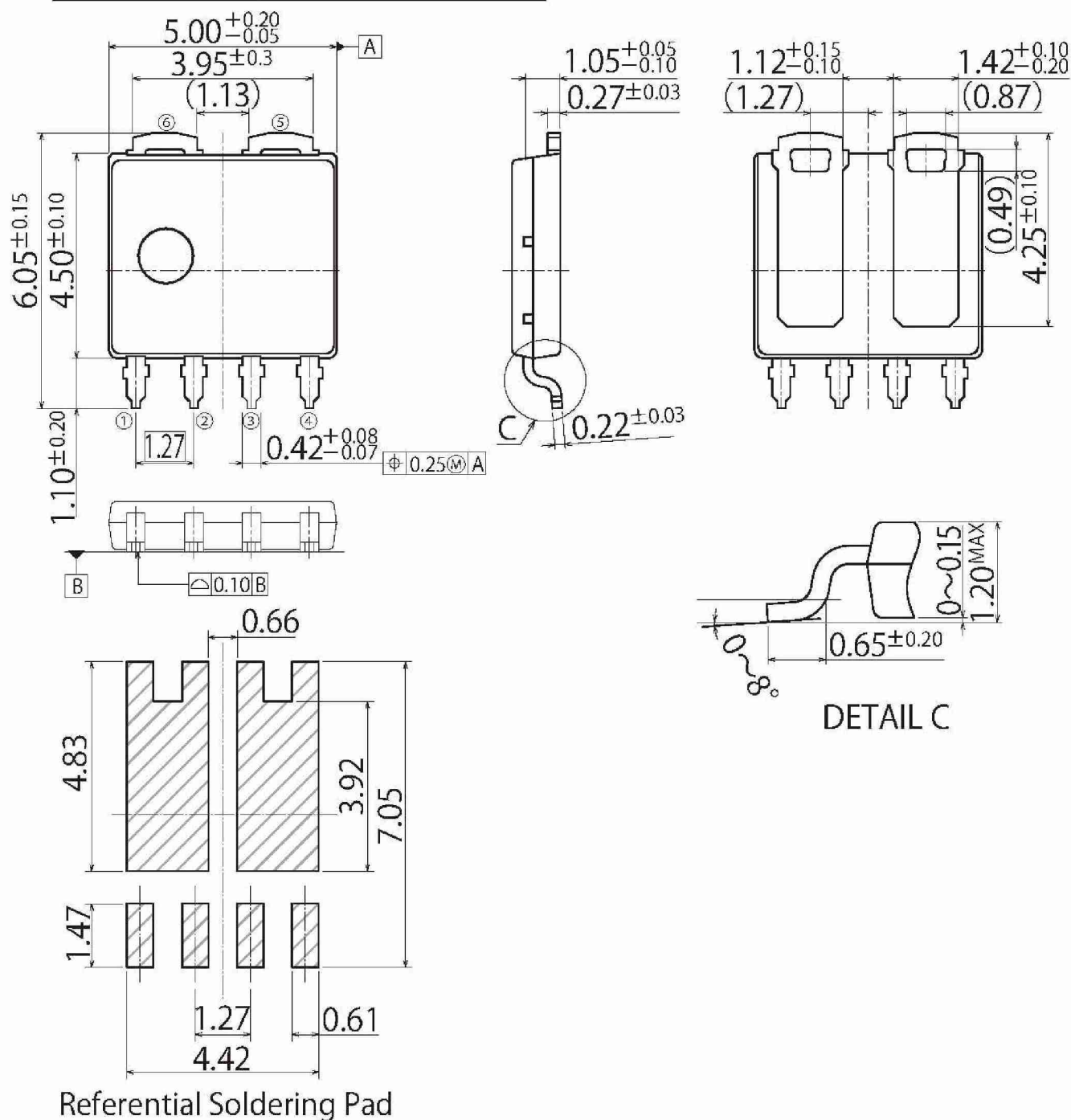


Single avalanche energy derating vs starting channel temperature



G8

JEDEC Code	—
JEITA Code	—
House Name	LF_Dual



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