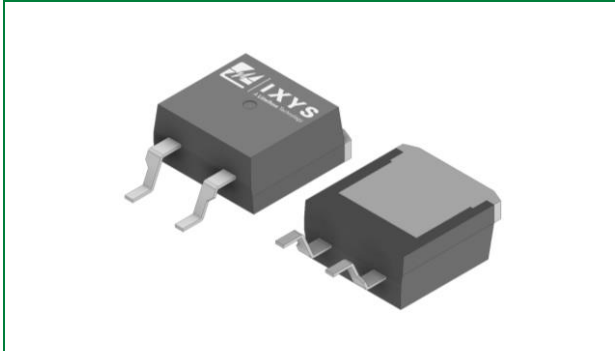


## LSIC2SD120D20A 1200 V, 20 A SiC Schottky Barrier Diode

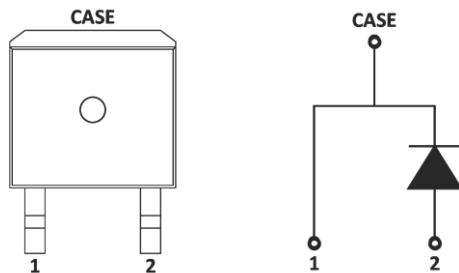


### Agency Approvals and Environmental

Environmental Approvals



### Pinout Diagram TO-263-2L



### Product Summary

Characteristic	Value	Unit
$V_{RRM}$	1200	V
$I_F (T_C \leq 135\text{ }^\circ\text{C})$	26	A
$Q_C (V_R: 0-800\text{ V})$	125	nC

### Features

- AEC-Q101 Qualified
- MSL1 Rated
- Positive temperature coefficient for safe operation and ease of paralleling
- 175 °C maximum operating junction temperature
- Excellent surge capability
- Extremely fast, temperature-independent switching behavior
- Dramatically reduced switching losses compared to Si bipolar diodes
- RoHS compliant, lead-free, and halogen-free

### Applications

- Boost diodes in PFC or DC/DC stages
- Switch-mode power supplies
- Solar inverters
- Uninterruptable power supplies
- Industrial motor drives
- Battery chargers
- High speed rectifier

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### 1. Maximum Ratings

Characteristic	Symbol	Conditions	Value	Unit
Repetitive Peak Reverse Voltage	$V_{RRM}$	-	1200	V
DC Blocking Voltage	$V_R$	-	1200	V
Continuous Forward Current	$I_F$	$T_C = 25\text{ }^\circ\text{C}$	55	A
		$T_C = 135\text{ }^\circ\text{C}$	26	
		$T_C = 149\text{ }^\circ\text{C}$	20	
Non-repetitive Forward Surge Current	$I_{FSM}$	$T_C = 25\text{ }^\circ\text{C}$ , $t_p = 10\text{ ms}$ , Half sine pulse	145	A
$I^2t$	$\int I^2 dt$	$T_C = 25\text{ }^\circ\text{C}$ , $t_p = 10\text{ ms}$ , Half sine pulse	105	A <sup>2</sup> s
Power Dissipation	$P_{Tot}$	$T_C = 25\text{ }^\circ\text{C}$	250	W
		$T_C = 110\text{ }^\circ\text{C}$	108	
Operating Junction Temperature	$T_J$	-	-55 to 175	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-	-55 to 150	$^\circ\text{C}$
Lead Temperature for Soldering (MSL 1 Rated)	$T_{SOLD}$	-	260	$^\circ\text{C}$

### 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Maximum Thermal Resistance, junction-to-case	$R_{thJC, max}$	0.6	$^\circ\text{C/W}$

### 3. Electrical Characteristics

Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Forward Voltage	$V_F$	$I_F = 20\text{ A}$ , $T_J = 25\text{ }^\circ\text{C}$	-	1.5	1.8	V
		$I_F = 20\text{ A}$ , $T_J = 175\text{ }^\circ\text{C}$	-	2.1	-	
Reverse Current	$I_R$	$V_R = 1200\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-	<1	100	$\mu\text{A}$
		$V_R = 1200\text{ V}$ , $T_J = 175\text{ }^\circ\text{C}$	-	8	-	
Total Capacitance	C	$V_R = 1\text{ V}$ , $f = 1\text{ MHz}$	-	1310	-	$\text{pF}$
		$V_R = 400\text{ V}$ , $f = 1\text{ MHz}$	-	120	-	
		$V_R = 800\text{ V}$ , $f = 1\text{ MHz}$	-	86	-	
Total Capacitive Charge	$Q_C$	$V_R = 800\text{ V}$ , $Q_C = \int C(V) dV$	-	125	-	nC
Capacitance Stored Energy	$E_C$	$V_R = 800\text{ V}$	-	28	-	$\mu\text{J}$

4. Performance Curves

Figure 1. Typical Forward Characteristics

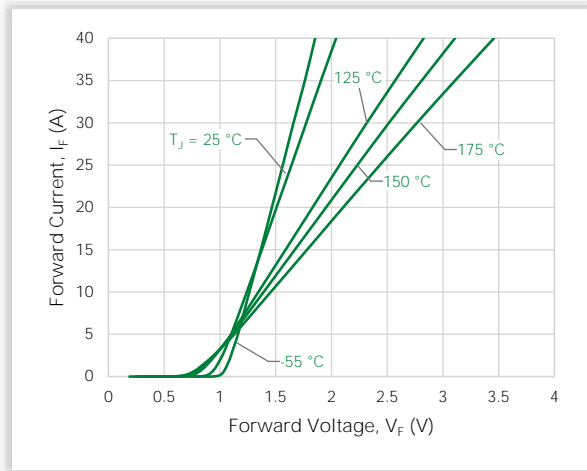


Figure 2. Typical Reverse Characteristics

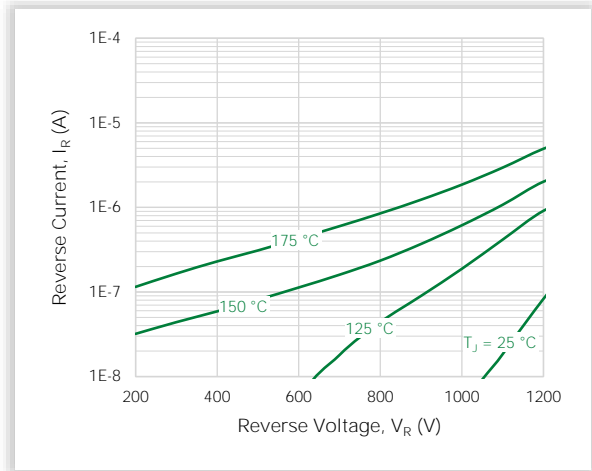


Figure 3. Power Derating

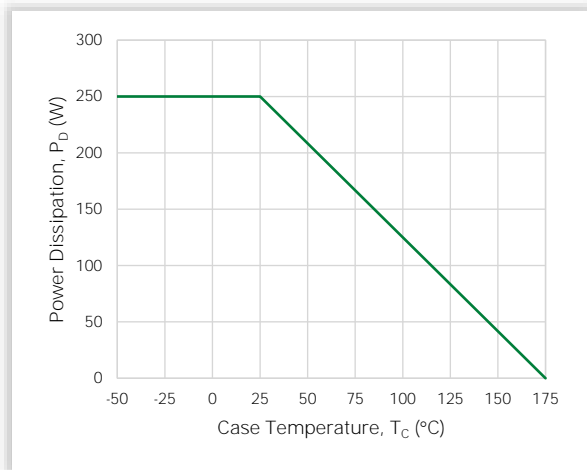


Figure 4. Current Derating

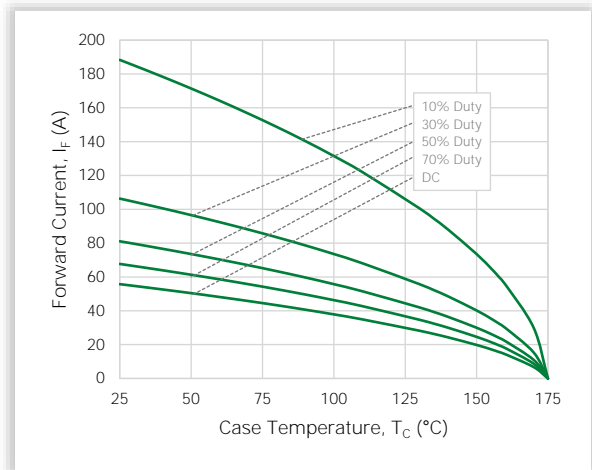


Figure 5. Capacitance vs. Reverse Voltage

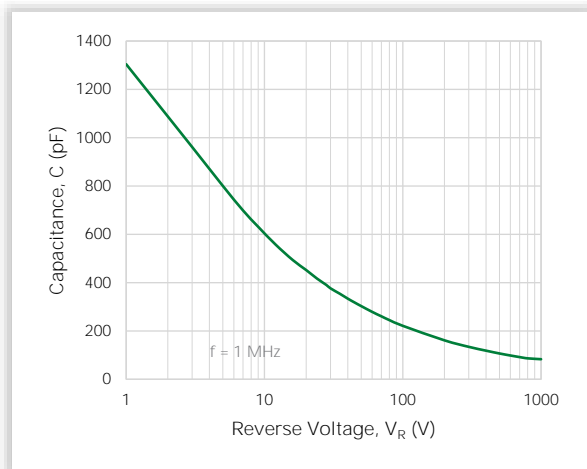


Figure 6. Capacitive Charge vs. Reverse Voltage

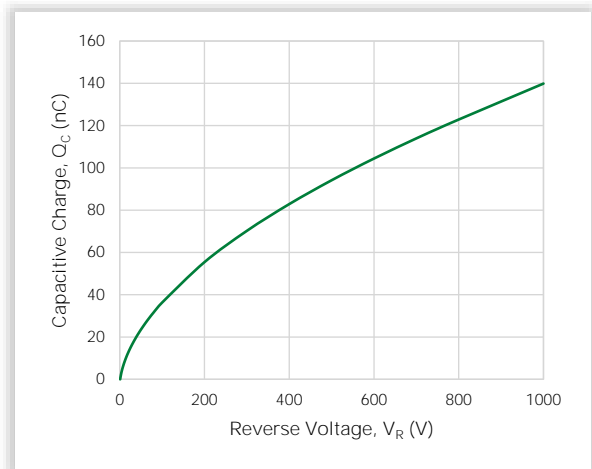


Figure 7. Stored Energy vs. Reverse Voltage

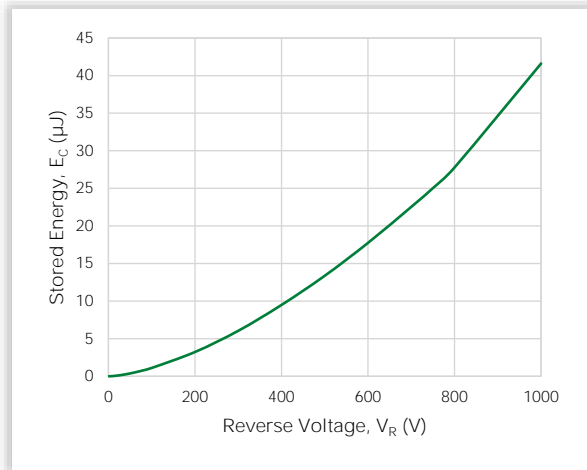
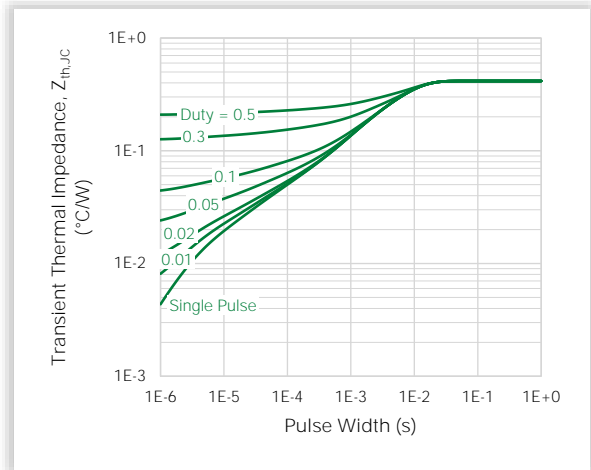
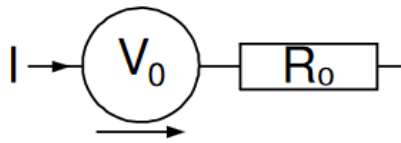


Figure 8. Transient Thermal Impedance



### 5. Diode V<sub>F</sub> Model for Simulation



$$V_F(T_J) = V_0 + IR_0$$

$$V_0 = -1.30 \times 10^{-3} \cdot T_J + 1.01 \times 10^0$$

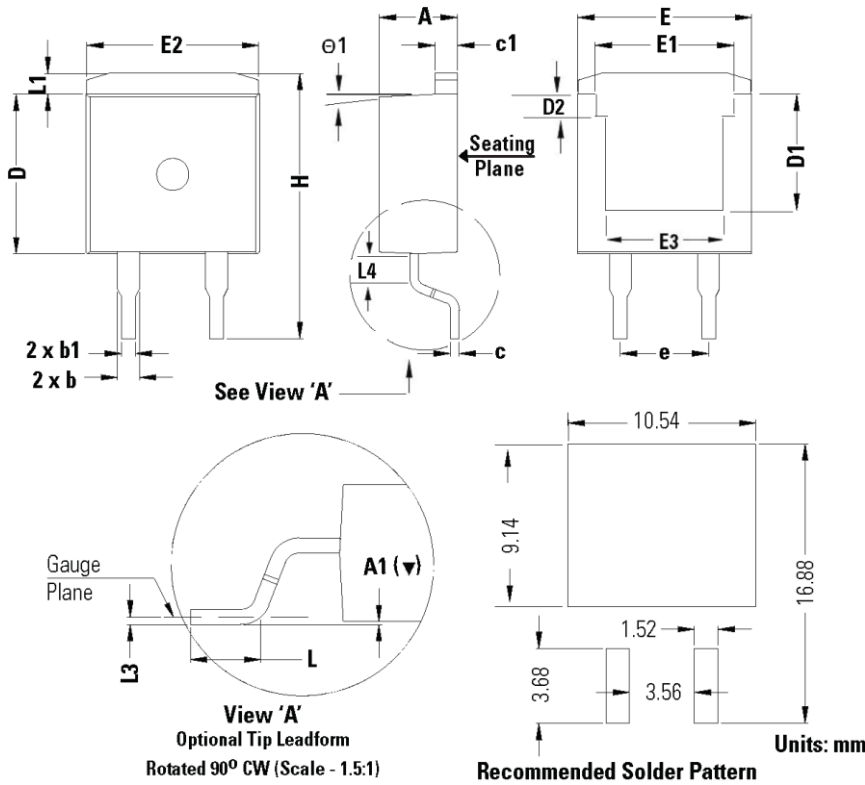
$$R_0 = 8.15 \times 10^{-7} \cdot T_J^2 + 1.03 \times 10^{-4} \cdot T_J + 2.36 \times 10^{-2}$$

Notes:

- T<sub>J</sub> is junction temperature in °C
- Range valid from 25 °C to 175 °C
- Model represents performance of a typical part

### 6. Package Dimensions

TO-263-2L Package

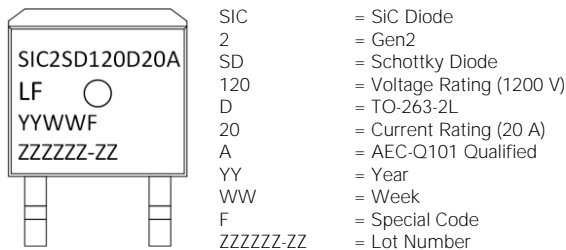


Symbol	Millimeters		
	Min	Nom	Max
A	4.30	4.60	4.70
A1(▼)	0.00	-	0.20
b	0.70	0.80	0.90
b1	1.18	1.28	1.38
c	0.45	0.50	0.60
c1	1.25	1.30	1.40
D	9.00	9.20	9.40
D1	6.70	6.90	7.10
D2	1.10	1.30	1.50
E	9.80	10.00	10.20
E1	8.20	8.40	8.60
E2	9.70	9.90	10.10
E3	7.80	8.00	8.20
e	5.08 BSC		
H	15.00	15.30	15.60
L	2.00	2.30	2.60
L1	1.00	1.20	1.40
L3	0.254 BSC		
L4	(2.00)		
Ø1	(3°)		

Notes:

1. These dimensions do not include protrusions of the mold.
2. The "( )" mark is the reference.
3. Coplanarity : Max 0.10mm
4. Metal finish – matte pure tin plating except trim area.
5. All plastic surfaces are polish finish.
6. Nominal 0.25 radius on all body edges and corners.

### 7. Part Numbering and Marking

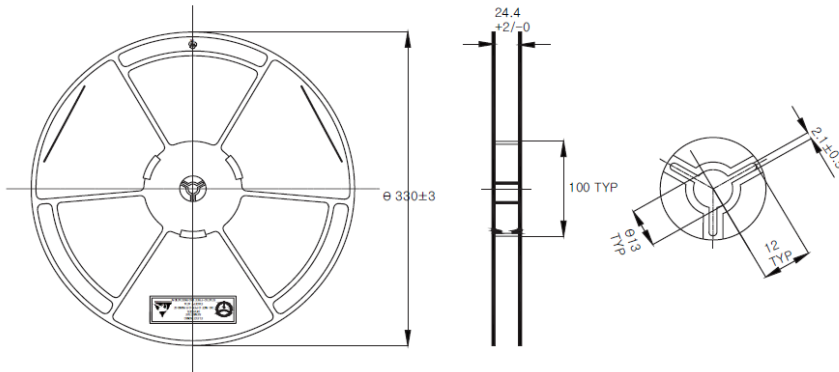
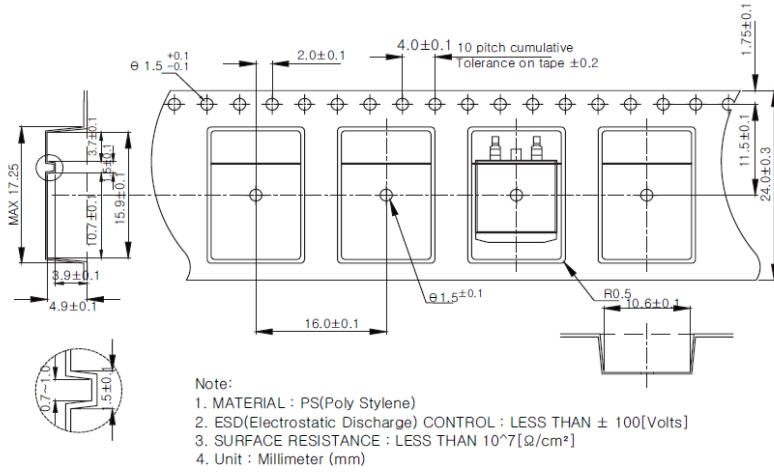


### 8. Packing Options

Part Number	Marking	Packing Mode	M.O.Q.
LSIC2SD120D20A	SIC2SD120D20A	Tape & Reel	800

### 9. Packing Specifications

#### TO-263 Carrier Tape and Reel Specifications



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