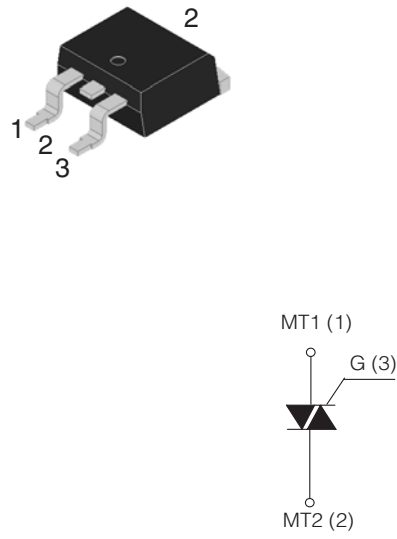



LOGIC LEVEL TRIAC

<p>TO-252AA (DPAK)</p> 	<p>On-State Current 8 Amp</p>	<p>Gate Trigger Current < 10 mA</p>	
	<p>Off-State Voltage 400 V ÷ 800 V</p>		
	<p>FEATURES</p> <ul style="list-style-type: none"> • Glass/passivated die junctions • Medium current Triac • Ideal for automated placement • Low thermal resistance • High surge current capability • Low forward voltage drop • Solder dip 260°C, 10s • Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC • Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C 		
	<p>MECHANICAL DATA</p> <ul style="list-style-type: none"> • Case: TO-252AA (DPAK). Epoxy meets UL 94V-0 flammability rating. • Polarity: As marked on the body. • Terminals: Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test. 		
<p>TYPICAL APPLICATIONS</p> <p>Logic level versions are designed to interface directly with low power drivers such as microcontrollers.</p>			

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95^\circ C$	8	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7$ ms)	84	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20$ ms)	80	A
I^2t	Fusing Current	$t_p = 10$ ms, Half Cycle	36	A ² s
I_{GM}	Peak Gate Current	20 μ s max. $T_j = 125^\circ C$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ C$	1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$, $t_r \leq 100$ ns $f = 120$ Hz, $T_j = 125^\circ C$	50	A/ μ s
T_j	Operating Temperature		(-40 +125)	°C
T_{stg}	Storage Temperature		(-40 +150)	°C
T_{sld}	Soldering Temperature	10s max	260	°C

SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	400	600	800	V

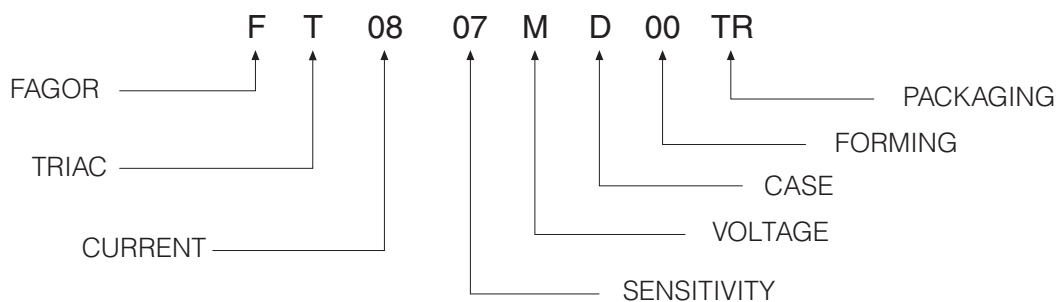
LOGIC LEVEL TRIAC
Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY		Unit
					07	08	
I _{GT} ⁽¹⁾	Gate Trigger Current	V _D = 12 V _{DC} , R _L = 33 Ω, T _j = 25 °C	Q1÷Q3	MAX	5	10	mA
			Q4	MAX	7		mA
V _{GT}	Gate Trigger Voltage	V _D = 12 V _{DC} , R _L = 33 Ω, T _j = 25 °C	Q1÷Q3	MAX		1.3	V
			Q1÷Q4	MAX	1.3		V
V _{GD}	Gate Non Trigger Voltage	V _D = V _{DRM} , R _L = 3.3 KΩ, T _j = 125 °C	Q1÷Q3	MIN		0.2	V
			Q1÷Q4	MIN	0.2		V
I _H ⁽²⁾	Holding Current	I _T = 100 mA, Gate open, T _j = 25 °C		MAX	15	15	mA
I _L	Latching Current	I _G = 1.2 I _{GT} , T _j = 25 °C	Q1,Q3	MAX	20	25	mA
			Q4	MAX	20		mA
			Q2,Q3,Q4	MAX	20	25	mA
			Q2	MAX	30	30	mA
dV/dt ⁽²⁾	Critical Rate of Voltage Rise	V _D = 0.67 x V _{DRM} , Gate open T _j = 125 °C		MIN	20	40	V/μs
(di/dt) _c ⁽²⁾	Critical Rate of Current Rise	(dv/dt) _c = 0.1 V/μs T _j = 125 °C		MIN	3.5	5.4	A/ms
		(dv/dt) _c = 10 V/μs T _j = 125 °C		MIN	1.5	2.8	A/ms
		without snubber T _j = 125 °C		MIN	-	-	
V _{TM} ⁽²⁾	On-state Voltage	I _T = 5.5 Amp, t _p = 380 μs, T _j = 25 °C		MAX	1.55		V
V _{to} ⁽²⁾	Threshold Voltage	T _j = 125 °C		MAX	0.85		V
r _d ⁽²⁾	Dynamic resistance	T _j = 125 °C		MAX	50		mΩ
I _{DRM} /I _{RRM}	Off-State Leakage Current	V _D = V _{DRM} , T _j = 125 °C		MAX	1		mA
		V _R = V _{RRM} , T _j = 25 °C		MAX	5		μA
R _{th(j-c)}	Thermal Resistance Junction-Case	for AC 360° conduction angle			1.6		°C/W
R _{th(j-a)}	Thermal Resistance Junction-Ambient	S ⁽³⁾ = 0.5cm ²			70		°C/W

(1) Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

(3) S: Cooper surface under tab.

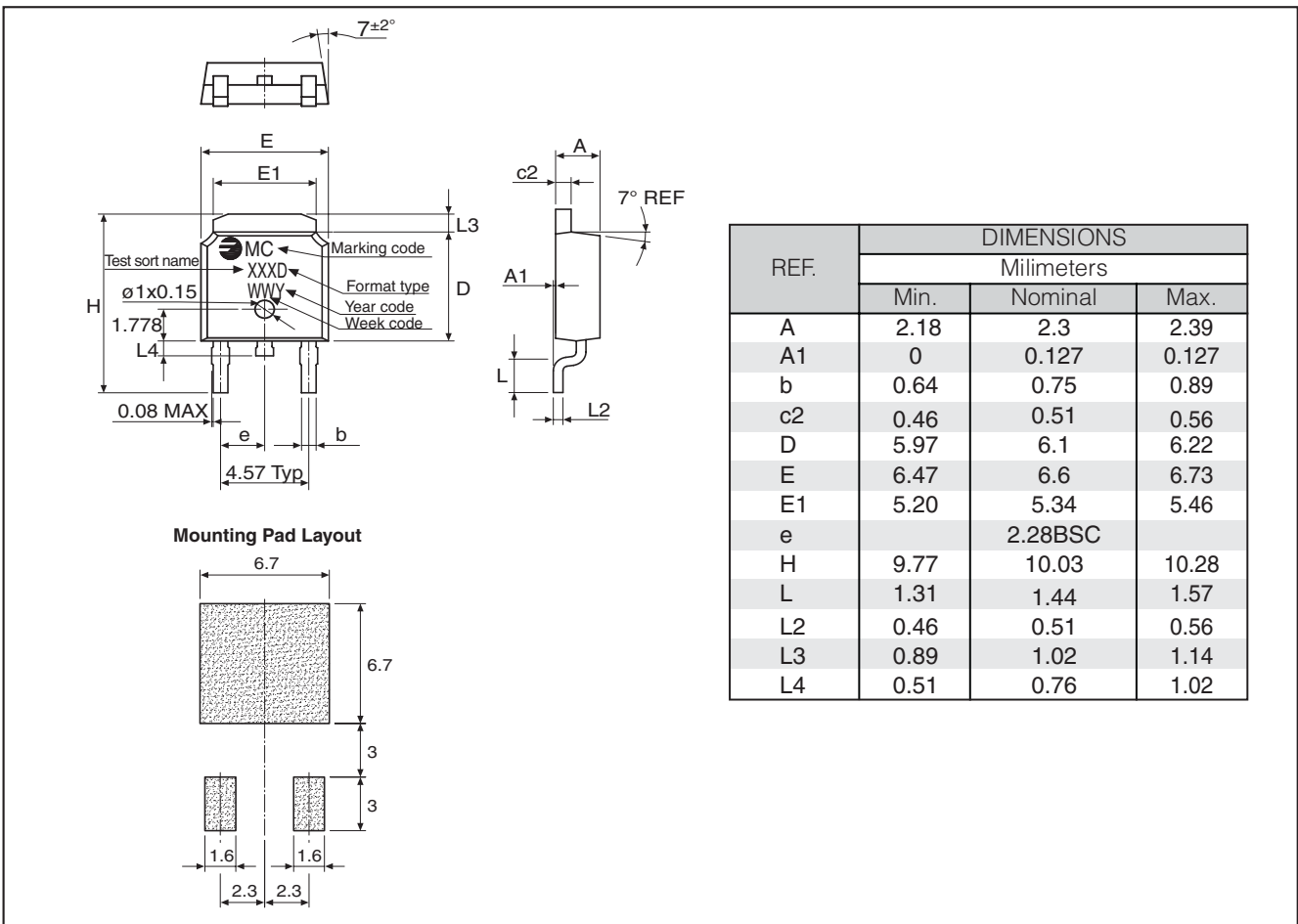
Part Number Information


LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0807MD 00TR	TR	13" diameter tape and reel	2,500	0.30

Package Outline Dimensions: (mm) TO-252AA (DPAK)



LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

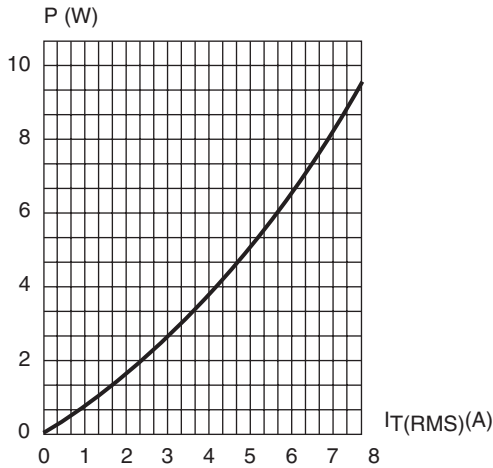


Fig. 2: RMS on-state current versus case temperature (full cycle).

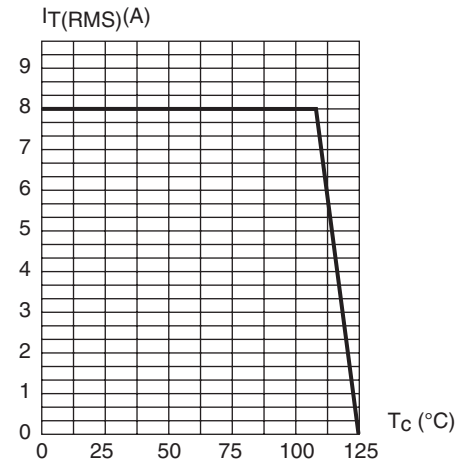


Fig. 3: Relative variation of thermal impedance versus pulse duration.

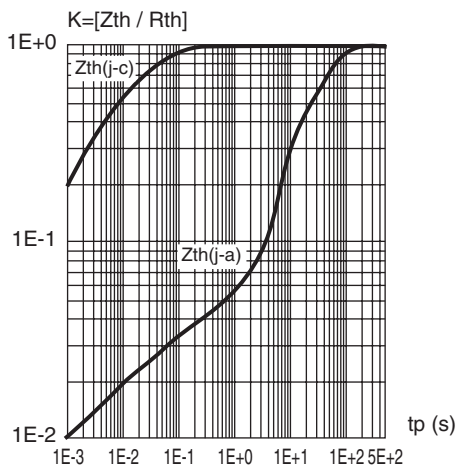


Fig. 4: On-state characteristics (maximum values)

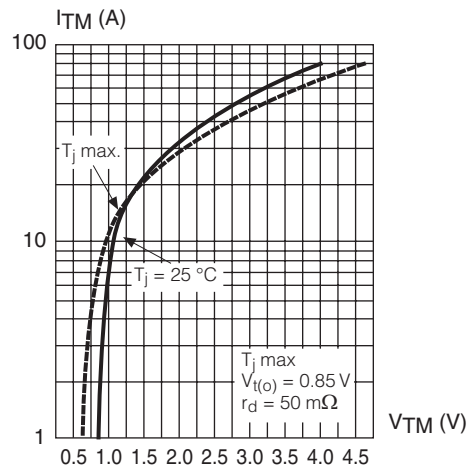


Fig. 5: Surge peak on-state current versus number of cycles

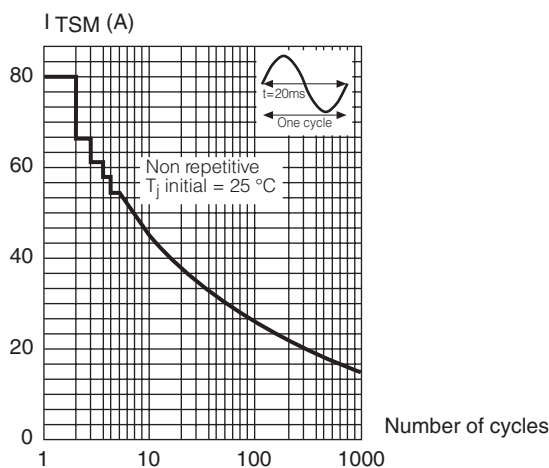
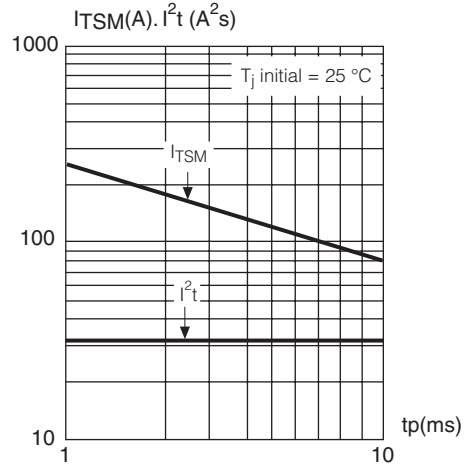


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.



LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

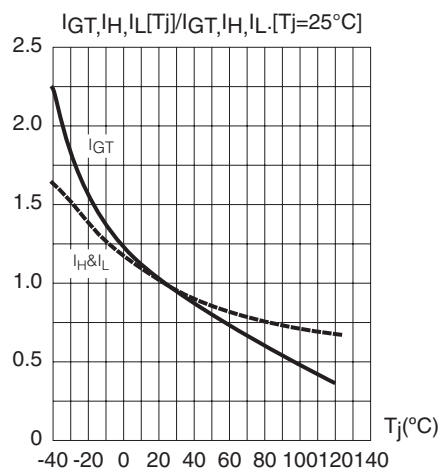


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

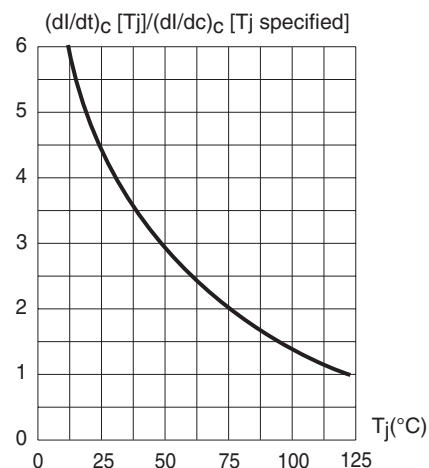
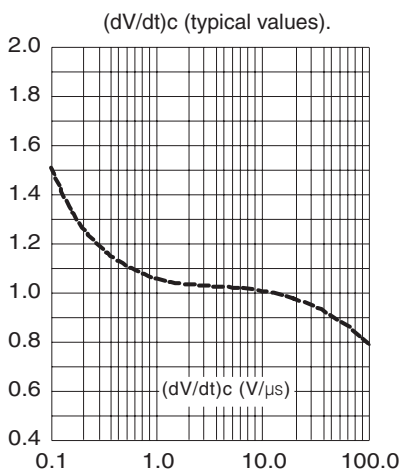


Fig. 9: Relative variation of critical rate of decrease of main current versus



LOGIC LEVEL TRIAC
Revision History

Date	Revision	Description of Changes
14-Sep-2009	0	Original Data Sheet
24-May-2013	1	200V and 700V eliminated
28-Mar-2017	2	Changed values of: I_{TSM} / I^2t / V_{GT} / V_{GD} / I_L / V_{TM} / r_d / I_{DRM}/I_{RRM}

Disclaimer

All product, product specifications and data are subject to change without notice to improve reliability, function or design or otherwise.

Fagor Electrónica, S.Coop., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Fagor"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Fagor makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Fagor disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Fagor's knowledge of typical requirements that are often placed on Fagor products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Fagor's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Fagor products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Fagor product could result in personal injury or death. Customers using or selling Fagor products not expressly indicated for use in such applications do so at their own risk and agree to fully indemnify and hold Fagor and its distributors harmless from and against any and all claims, liabilities, expenses and damages arising or resulting in connection with such use or sale, including attorneys fees, even if such claim alleges that Fagor or its distributor was negligent regarding the design or manufacture of the part. Please contact authorized Fagor personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Fagor, Product names and markings noted herein may be trademarks of their respective owners.