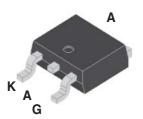
RoHS



SENSITIVE GATE SCR

TO-252AA (DPAK)



On-State Current

Gate Trigger Current

4 Amp

<200 µA

Off-State Voltage

400 V ÷ 800 V

FEATURES

- Glass/passivated die junctions
- Low current SCR
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C



- Case: TO-252AA (DPAK). Epoxy meets UL 94V-0 flammability rating.
- Polarity: As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.



TYPICAL APPLICATIONS

Thanks to highly sensitive triggering levels, the FS04xxxD SCR series is suitable for all applications where available gate current is limited, such as ground fault circuit interruptors, pilot circuits in solid state relays, stand-by mode power supplies, smoke and alarm detectors.

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
I _{T(RMS)}	On-state Current	180 ° Conduction Angle, T _C = 110 °C	4	А
I _{T(AV)}	Average On-state Current	180 ° Conduction Angle, T _C = 110 °C	2.5	А
I _{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	33	А
I _{TSM}	Non-repetitive On-State Current	Halfl Cycle, 50 Hz	30	А
I ² t	Fusing Current	tp = 10 ms, Half Cycle	4.5	A ² s
I _{GM}	Peak Gate Current	20 μs max.	1.2	А
P _{GM}	Peak Gate Dissipation	20 μs max.	3	W
P _{G(AV)}	Gate Dissipation	20ms max.	0.2	W
T _j	Operating Temperature		(-40 to +125)	°C
T _{stg}	Storage Temperature		(-40 to +150)	°C
T _{sld}	Soldering Temperature	10s max.	260	°C
V_{RGM}	Reverse Gate Voltage		5	V

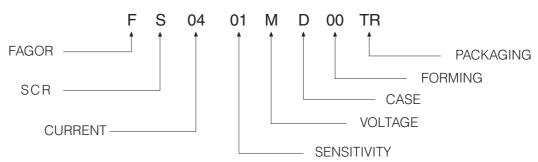
SYMBOL	PARAMETER	CONDITIONS		Unit		
01111202	T A T A T A T A T A T A T A T A T A T A	CONDITIONS	D	M	N	
$V_{\text{DRM}} \ V_{\text{RRM}}$	Repetitive Peak Off State Voltage	$R_{GK} = 1 k\Omega$	400	600	800	V



Electrical Characteristics at Tamb = 25 °C

SYMBOL PARAMETER		CONDITIONS		SENSITIVITY			11		
STWIDOL	FARAMLILA	CONDITIONS			01	02	03	04	Unit
I _{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 140 \Omega$. T _j = 25 °C	MIN	1		20	15	μΑ
				MAX	20	200	200	50	
V _{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 140 \Omega.$	$T_j = 25 ^{\circ}C$	MAX	0.8			V	
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3 \text{ k}\Omega,$	R_{GK} = 220 Ω	MIN		0	.1		V
		T _j = 125 °C							
V_{RGM}	Reverse Gate Voltage	$I_{RG} = 10\mu A$,		MIN	8			V	
I _H	Holding Current	$I_T = 50 \text{ mA}, R_{GK} = 1 \text{ k}\Omega$	$T_j = 25 ^{\circ}C$	MAX	5			mA	
IL	Latching Current	I_G = 1 mA, R_{GK} = 1 k Ω		MAX	6			mA	
dV/dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, R_{GK} = 0.67 \times V_{DRM}$	1 kΩ,	MIN	10	5	10	10	V/µs
		T _j = 125 °C			10	5	10	10	
dI/dt	Critical Rate of Current Rise	$I_{G} = 2 \times I_{GT} \text{ tr} \le 100 \text{ ns}, f = 60 \text{ Hz}, MIN 50$			A/µs				
		T _j = 125 °C							
V_{TM}	On-state Voltage	at $I_T = 8$ Amp, tp = 380 μ s, $T_j = 25$ °C MAX 1.6			V				
V _{t 0}	Threshold Voltage	$T_j = 125 ^{\circ}\text{C}$ MAX 0.85		85		V			
r _d	Dynamic resistance	$T_j = 125 ^{\circ}\text{C}$		MAX	90			m Ω	
I _{DRM} /I _{RRM}	Off-State Leakage Current	$V_D = V_{DRM}, R_{GK} = 1k\Omega$ $T_j = 125 °C$ MAX			mA				
		$V_R = V_{RRM}$, $T_j = 25 ^{\circ}C$		MAX	5			μΑ	
R _{th(j-c)}	Thermal Resistance	for AC 360° conduction angle 1.6			°C/W				
	Junction-Amb for DC								
R _{th(j-a)}	Thermal Resistance	$S = 1 cm^2 $ 70			°C/W				
	Junction-Amb for DC								

Part Number Information

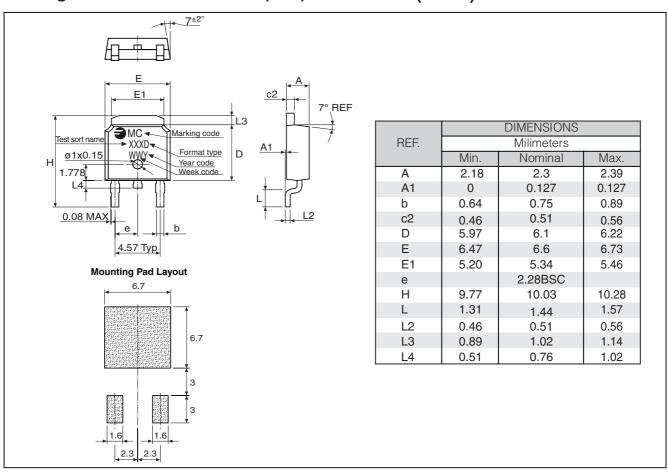




Ordering information

PREFERRED P/N PACKAGE CODE		DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)	
FS0401MD 00TR	TR	13" diameter tape and reel	2,500	0.30	

Package Outline Dimensions: (mm) TO-252AA (DPAK)



Revision: 1



Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum average power dissipation versus average on-state current.

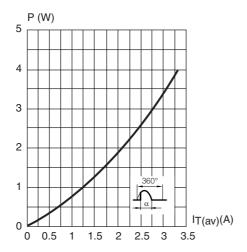


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration.

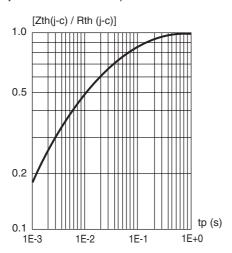


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).

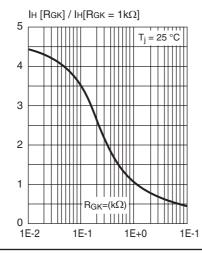


Fig. 2: Average and D.C. on-state current versus case temperature.

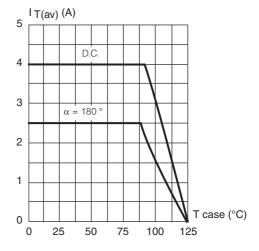


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

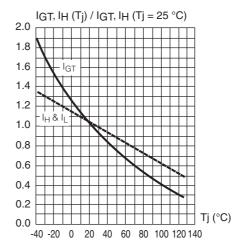
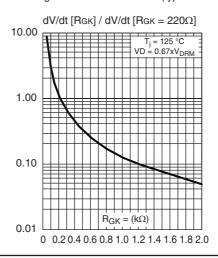


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).





Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Revision: 1

Fig. 7: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

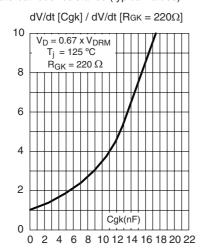


Fig. 9: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.

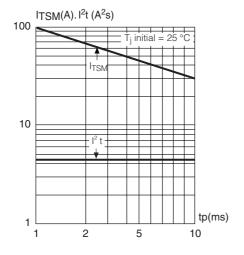


Fig. 8: Non repetitive surge peak on-state current versus number of cycles.

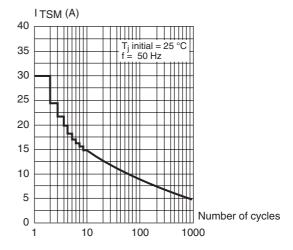
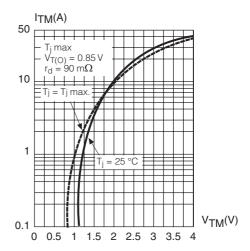


Fig. 10: On-state characteristics (maximum values).





Revision History

Date Revision		Description of Changes		
14-Sep-2009	0	Original Data Sheet		
20-Jan-2017 1		200V and 700V eliminated		

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Revision: 1