

# High Efficiency Thyristor

$$V_{RRM} = 2 \times 1200 \text{ V}$$

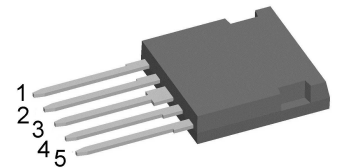
$$I_{TAV} = 40 \text{ A}$$

$$V_T = 1,19 \text{ V}$$

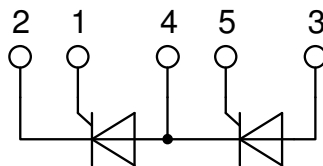
Phase leg

Part number

**CLA40P1200FC**



Backside: isolated



### Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

### Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

### Package: i4-Pac

- Isolation Voltage: 3000 V~
- Industry convenient outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Soldering pins for PCB mounting
- Backside: DCB ceramic
- Reduced weight
- Advanced power cycling

### Terms .Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact the sales office, which is responsible for you.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you.

Should you intend to use the product in aviation, in health or live endangering or life support applications, please notify. For any such application we urgently recommend

- to perform joint risk and quality assessments;

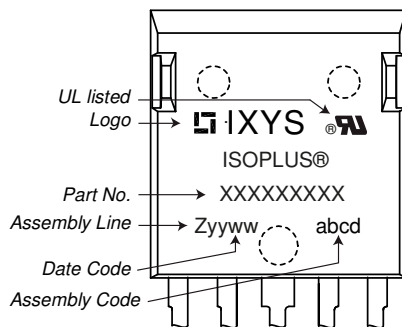
- the conclusion of quality agreements;

- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
$I_{RD}$	reverse current, drain current	$V_{R/D} = 1200 V$	$T_{VJ} = 25^{\circ}C$		50	$\mu A$
		$V_{R/D} = 1200 V$	$T_{VJ} = 125^{\circ}C$		4	mA
$V_T$	forward voltage drop	$I_T = 40 A$	$T_{VJ} = 25^{\circ}C$		1,25	V
		$I_T = 80 A$			1,49	V
		$I_T = 40 A$	$T_{VJ} = 125^{\circ}C$		1,19	V
		$I_T = 80 A$			1,50	V
$I_{TAV}$	average forward current	$T_C = 95^{\circ}C$	$T_{VJ} = 150^{\circ}C$		40	A
$I_{T(RMS)}$	RMS forward current	180° sine			63	A
$V_{T0}$	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0,86	V
$r_T$	slope resistance				7,9	m $\Omega$
$R_{thJC}$	thermal resistance junction to case				0,8	K/W
$R_{thCH}$	thermal resistance case to heatsink			0,20		K/W
$P_{tot}$	total power dissipation		$T_C = 25^{\circ}C$		150	W
$I_{TSM}$	max. forward surge current	$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 45^{\circ}C$		650	A
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		700	A
		$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 150^{\circ}C$		555	A
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		595	A
$I^2t$	value for fusing	$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 45^{\circ}C$		2,12	kA <sup>2</sup> s
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		2,04	kA <sup>2</sup> s
		$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 150^{\circ}C$		1,54	kA <sup>2</sup> s
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		1,48	kA <sup>2</sup> s
$C_J$	junction capacitance	$V_R = 400 V \quad f = 1 MHz$	$T_{VJ} = 25^{\circ}C$		25	pF
$P_{GM}$	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
$P_{GAV}$	average gate power dissipation				0,5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50 Hz$	repetitive, $I_T = 120 A$		150	A/ $\mu s$
		$t_p = 200 \mu s; di_G/dt = 0,3 A/\mu s;$ $I_G = 0,3 A; V = \frac{2}{3} V_{DRM}$	non-repet., $I_T = 40 A$		500	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; \text{method 1 (linear voltage rise)}$	$T_{VJ} = 150^{\circ}C$		1000	V/ $\mu s$
$V_{GT}$	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1,5	V
			$T_{VJ} = -40^{\circ}C$		1,6	V
$I_{GT}$	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		50	mA
			$T_{VJ} = -40^{\circ}C$		80	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0,2	V
$I_{GD}$	gate non-trigger current				3	mA
$I_L$	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		125	mA
		$I_G = 0,3 A; di_G/dt = 0,3 A/\mu s$				
$I_H$	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	$\mu s$
		$I_G = 0,3 A; di_G/dt = 0,3 A/\mu s$				
$t_q$	turn-off time	$V_R = 100 V; I_T = 40 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		200	$\mu s$

Package i4-Pac			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$I_{RMS}$	RMS current	per terminal			70	A
$T_{VJ}$	virtual junction temperature		-40		150	°C
$T_{op}$	operation temperature		-40		125	°C
$T_{stg}$	storage temperature		-40		150	°C
<b>Weight</b>				9		g
$F_C$	mounting force with clip		20		120	N
$d_{Spp/App}$	creepage distance on surface / striking distance through air	terminal to terminal	1,7			mm
$d_{Spb/Apb}$		terminal to backside	5,1			mm
$V_{ISOL}$	isolation voltage	t = 1 second	3000			V
		t = 1 minute	2500			V

### Product Marking



### Part description

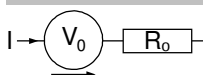
- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 40 = Current Rating [A]
- P = Phase leg
- 1200 = Reverse Voltage [V]
- FC = i4-Pac (5)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA40P1200FC	CLA40P1200FC	Tube	25	510210

### Equivalent Circuits for Simulation

\* on die level

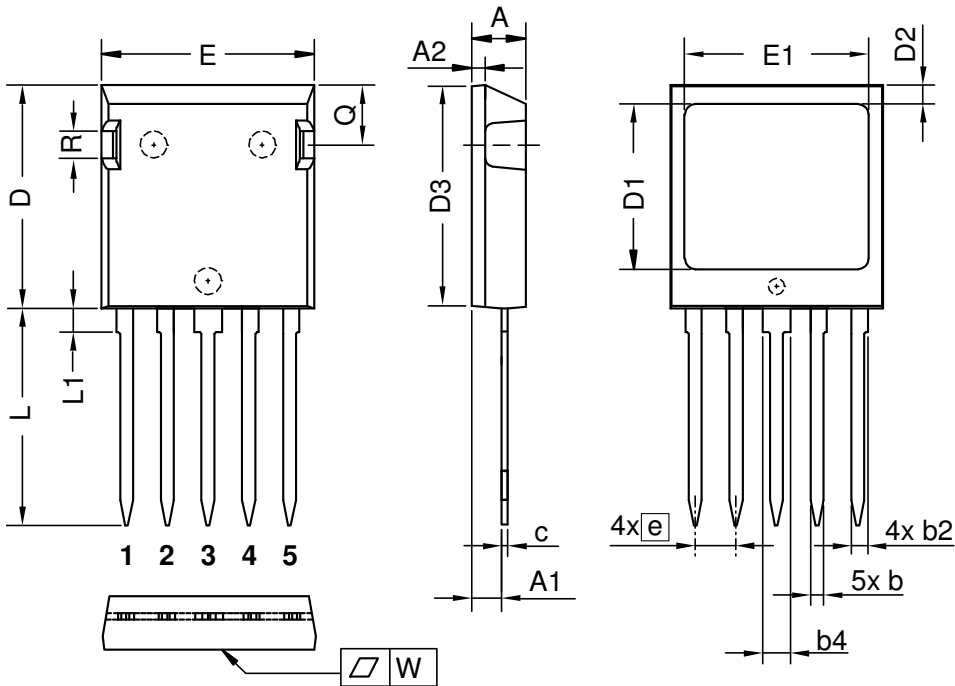
$T_{VJ} = 150\text{ °C}$



Thyristor

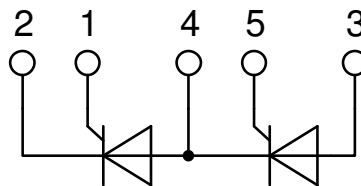
$V_{0\ max}$	threshold voltage	0,86	V
$R_{0\ max}$	slope resistance *	5,4	mΩ

## Outlines i4-Pac



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.83	5.21	0.190	0.205
A1	2.59	3.00	0.102	0.118
A2	1.17	2.16	0.046	0.085
b	1.14	1.40	0.045	0.055
b2	1.47	1.73	0.058	0.068
b4	2.54	2.79	0.100	0.110
c	0.51	0.74	0.020	0.029
D	20.80	21.34	0.819	0.840
D1	14.99	15.75	0.590	0.620
D2	1.65	2.03	0.065	0.080
D3	20.30	20.70	0.799	0.815
E	19.56	20.29	0.770	0.799
E1	16.76	17.53	0.660	0.690
e	3.81 BSC		0.150 BSC	
L	19.81	21.34	0.780	0.840
L1	2.11	2.59	0.083	0.102
Q	5.33	6.20	0.210	0.244
R	2.54	4.57	0.100	0.180
W	-	0.10	-	0.004

Die konvexe Form des Substrates ist typ. < 0.05 mm über der Kunststoffoberfläche der Bauteilunterseite  
 The convexbow of substrate is typ. < 0.05 mm over plastic surface level of device bottom side



## Thyristor

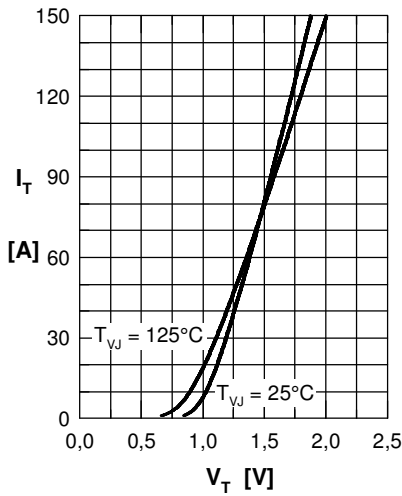


Fig. 1 Forward characteristics

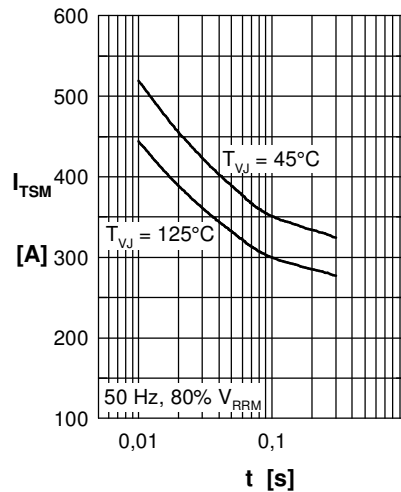


Fig. 2 Surge overload current  
 $I_{TSM}$ : crest value,  $t$ : duration

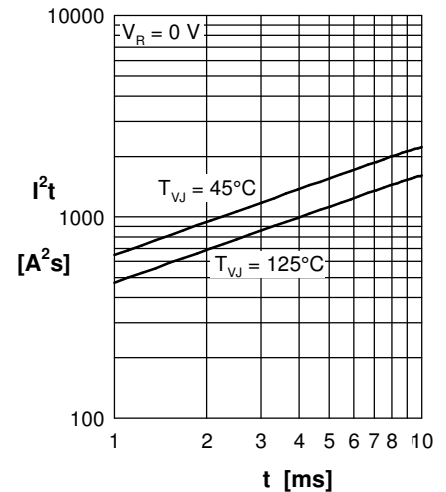


Fig. 3  $I^2t$  versus time (1-10 s)

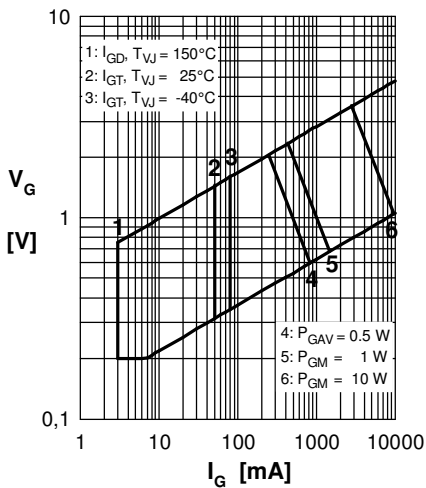


Fig. 4 Gate voltage & gate current

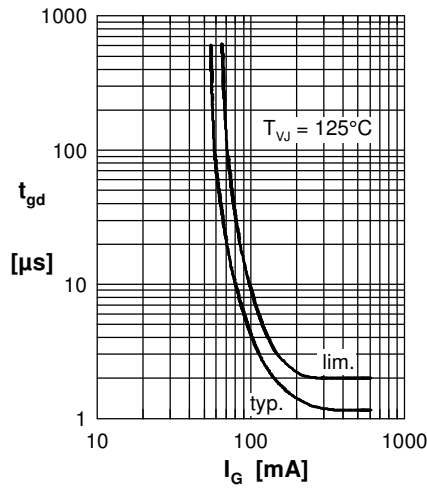


Fig. 5 Gate controlled delay time  $t_{gd}$

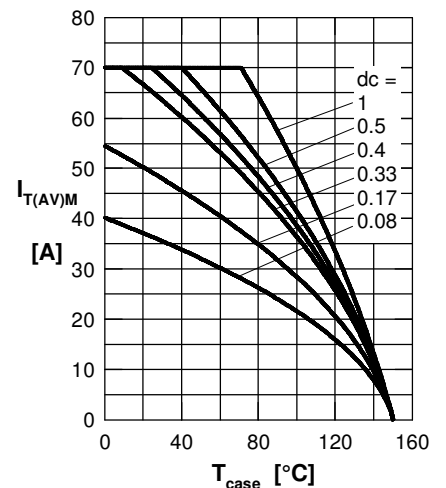


Fig. 6 Max. forward current at case temperature

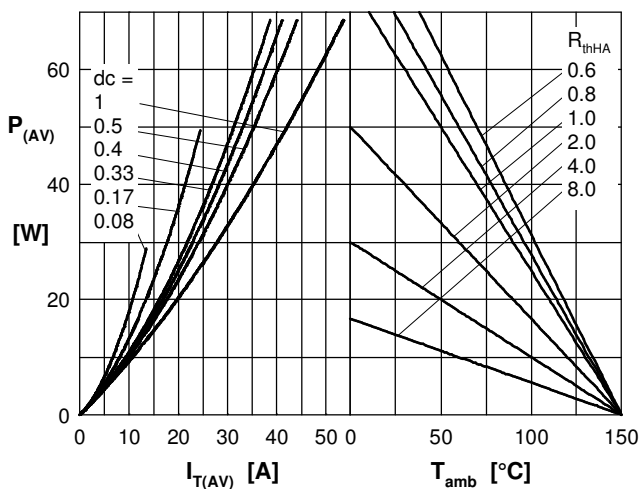


Fig. 7a Power dissipation versus direct output current  
Fig. 7b and ambient temperature

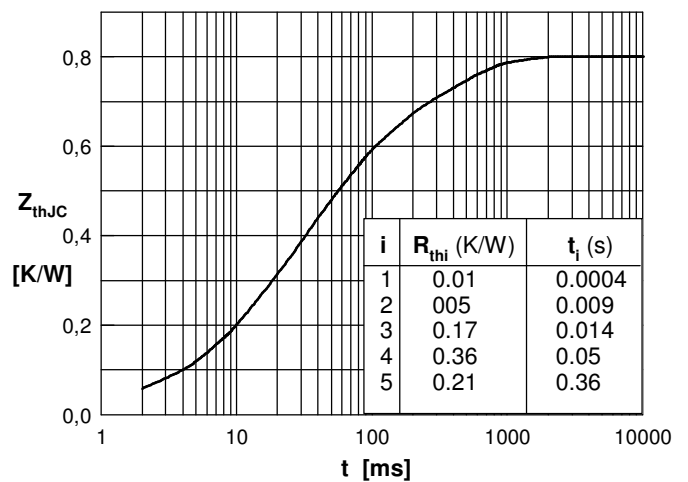


Fig. 7 Transient thermal impedance junction to case