# CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

## High-Speed CMOS Logic, 3- to 8-Line Decoder/Demultiplexer with Address Latches

## Features

- **Select One of Eight Data Outputs**
  - **Active Low for CD74HC137 and CD74HCT137**
  - **Active High for 'HC237 and CD74HCT237**

- **I/O Port or Memory Selector**

- **Two Enable Inputs to Simplify Cascading**

- **Typical Propagation Delay of 13ns at $V_{CC}$ = 5V, 15pF, $T_A$ = 25$^o$C (CD74HC237)**

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . . . . . . . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . . . . . . . . . 15 LSTTL Loads**

- **Wide Operating Temperature Range . . . -55$^o$C to 125$^o$C**

- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**

- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30%, of $V_{CC}$ at $V_{CC}$ = 5V**

- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$ = 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \le 1\mu A$ at $V_{OL}$, $V_{OH}$**

## Description

The CD74HC137, CD74HCT137, 'HC237, and CD74HCT237 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

Both circuits have three binary select inputs (A0, A1 and A2) that can be latched by an active High Latch Enable (LE) signal to isolate the outputs from select-input changes. A "Low" LE makes the output transparent to the input and the circuit functions as a one-of-eight decoder. Two Output Enable inputs ($\overline{OE}_1$ and $OE_0$) are provided to simplify cascading and to facilitate demultiplexing. The demultiplexing function is accomplished by using the $A_0$, $A_1$, $A_2$ inputs to select the desired output and using one of the other Output Enable inputs as the data input while holding the other Output Enable input in its active state. In the CD74HC137 and CD74HCT137 the selected output is a "Low"; in the 'HC237 and CD74HCT237 the selected output is a "High".
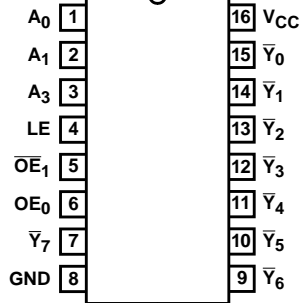
## Ordering Information

| PART NUMBER | TEMP. RANGE ($^o$C) | PACKAGE |
|---|---|---|
| CD54HC237F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC137E | -55 to 125 | 16 Ld PDIP |
| CD74HC137PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC137PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC137PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HC237E | -55 to 125 | 16 Ld PDIP |
| CD74HC237M | -55 to 125 | 16 Ld SOIC |
| CD74HC237MT | -55 to 125 | 16 Ld SOIC |
| CD74HC237M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC237NSR | -55 to 125 | 16 Ld SOP |
| CD74HC237PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC237PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC237PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HCT137E | -55 to 125 | 16 Ld PDIP |
| CD74HCT137MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT137M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT237E | -55 to 125 | 16 Ld PDIP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.
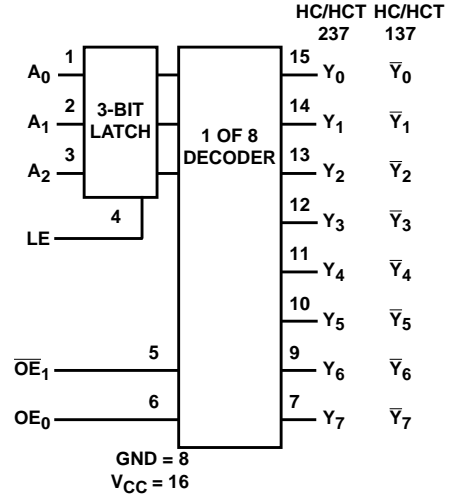
# CD74HC137, CD74HCT137, CD54HC237, CD74HC237, CD74HCT237

## *Pinout*

**CD54HC237 (CERDIP)**
**CD74HC137 (PDIP, TSSOP)**
**CD74HCT137 (PDIP, SOIC)**
**CD74HC237 (PDIP, SOIC, SOP, TSSOP)**
**CD74HCT237 (PDIP)**
TOP VIEW

| | | | |
|---|---|---|---|
| $A_0$ | 1 | 16 | $V_{CC}$ |
| $A_1$ | 2 | 15 | $\overline{Y}_0$ |
| $A_3$ | 3 | 14 | $\overline{Y}_1$ |
| LE | 4 | 13 | $\overline{Y}_2$ |
| $\overline{OE}_1$ | 5 | 12 | $\overline{Y}_3$ |
| $OE_0$ | 6 | 11 | $\overline{Y}_4$ |
| $\overline{Y}_7$ | 7 | 10 | $\overline{Y}_5$ |
| GND | 8 | 9 | $\overline{Y}_6$ |

## *Functional Diagram*

HC/HCT 237    HC/HCT 137

$A_0$ — 1 — 3-BIT LATCH — 1 OF 8 DECODER — 15 — $Y_0$ / $\overline{Y}_0$
$A_1$ — 2 — 14 — $Y_1$ / $\overline{Y}_1$
$A_2$ — 3 — 13 — $Y_2$ / $\overline{Y}_2$
LE — 4 — 12 — $Y_3$ / $\overline{Y}_3$
11 — $Y_4$ / $\overline{Y}_4$
10 — $Y_5$ / $\overline{Y}_5$
$\overline{OE}_1$ — 5 — 9 — $Y_6$ / $\overline{Y}_6$
$OE_0$ — 6 — 7 — $Y_7$ / $\overline{Y}_7$

GND = 8
$V_{CC}$ = 16

### 'HC137, 'HCT137 TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LE | $OE_0$ | $\overline{OE}_1$ | $A_2$ | $A_1$ | $A_0$ | $\overline{Y}_0$ | $\overline{Y}_1$ | $\overline{Y}_2$ | $\overline{Y}_3$ | $\overline{Y}_4$ | $\overline{Y}_5$ | $\overline{Y}_6$ | $\overline{Y}_7$ |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Depends upon the address previously applied while LE was at a logic low. | | | | | | | |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

### 'HC237, 'HCT237 TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LE | $OE_0$ | $\overline{OE}_1$ | $A_2$ | $A_1$ | $A_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| X | X | H | X | X | X | L | L | L | L | L | L | L | L |
| X | L | X | X | X | X | L | L | L | L | L | L | L | L |
| L | H | L | L | L | L | H | L | L | L | L | L | L | L |
| L | H | L | L | L | H | L | H | L | L | L | L | L | L |
| L | H | L | L | H | L | L | L | H | L | L | L | L | L |
| L | H | L | L | H | H | L | L | L | H | L | L | L | L |
| L | H | L | H | L | L | L | L | L | L | H | L | L | L |
| L | H | L | H | L | H | L | L | L | L | L | H | L | L |
| L | H | L | H | H | L | L | L | L | L | L | L | H | L |
| L | H | L | H | H | H | L | L | L | L | L | L | L | H |
| H | H | L | X | X | X | Depends upon the address previously applied while LE was at a logic low. | | | | | | | |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

**Functional Block Diagram**
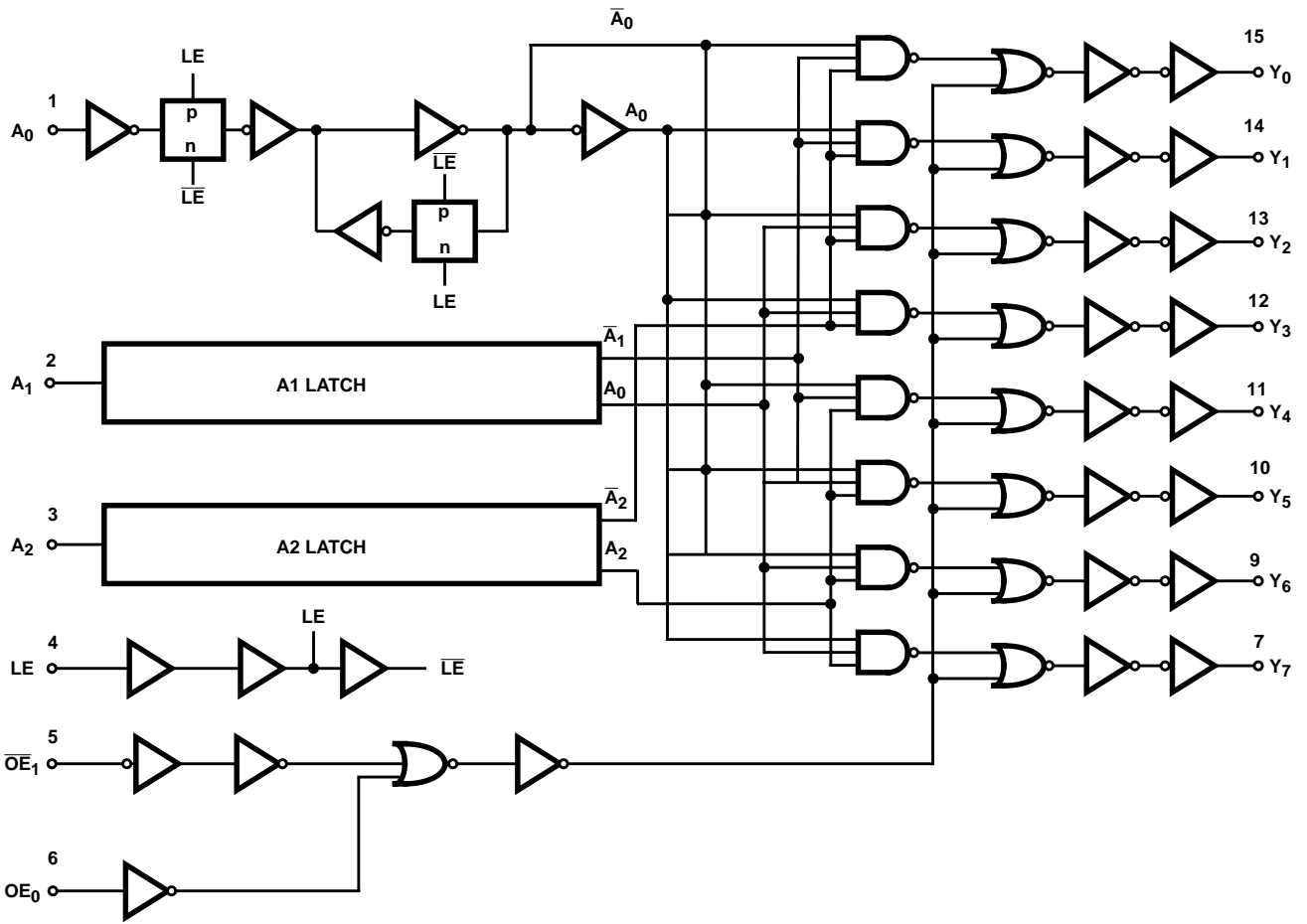
## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
  For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ . . . . . . . . . . . . . . . . . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
  For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ . . . . . . . . . . . . . . . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
  For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ . . . . . . . . . . . . . . . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . . . . . . . . . . . . . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
  HC Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .2V to 6V
  HCT Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . . . . . . . . . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
  2V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1000ns (Max)
  4.5V. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 500ns (Max)
  6V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 400ns (Max)

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 1):
  E (PDIP) Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .67°C/W
  M (SOIC) Package. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .73°C/W
  NS (SOP) Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .64°C/W
  PW (TSSOP) Package . . . . . . . . . . . . . . . . . . . . . . . . . . 108°C/W
Maximum Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . 150°C
Maximum Storage Temperature Range . . . . . . . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . 300°C
  (SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

 1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |

## DC Electrical Specifications    (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| All | 1.5 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | |
| $A_n$ to LE Setup Time | $t_{SU}$ | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | - | 11 | - | 13 | - | ns |
| $A_n$ to LE Hold Time | $t_H$ | 2 | 30 | - | - | 40 | - | 45 | - | ns |
| | | 4.5 | 6 | - | - | 8 | - | 9 | - | ns |
| | | 6 | 5 | - | - | 7 | - | 8 | - | ns |

**Prerequisite For Switching Specifications**   (Continued)

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| LE Pulse Width | $t_W$ | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | 6 | 9 | - | - | 1 | - | 13 | - | ns |
| **HCT TYPES** | | | | | | | | | | |
| An to LE Setup Time | $t_{SU}$ | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| An to LE Hold Time | | | | | | | | | | |
|    CD74HCT137 | $t_H$ | 4.5 | 7 | - | - | 9 | - | 11 | - | ns |
|    CD74HCT237 | $t_H$ | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| LE Pulse Width | $t_W$ | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay CD74HC137, CD74HCT137 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 180 | - | 225 | - | 270 | ns |
|    An to any $\overline{Y}$ | | | 4.5 | - | - | 36 | - | 45 | - | 54 | ns |
| | | | 6 | - | - | 31 | - | 38 | - | 46 | ns |
| Propagation Delay 'HC237, CD74HCT237 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 160 | - | 200 | - | 240 | ns |
|    An to any Y | | | 4.5 | - | - | 32 | - | 40 | - | 48 | ns |
| | | | 6 | - | - | 27 | - | 34 | - | 41 | ns |
|    Address to Output | | | | | | | | | | | |
|    CD74HC137 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 15pF | 5 | 5 | 15 | - | - | - | - | - | ns |
|    'HC237 | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 15pF | 5 | - | 13 | - | - | - | - | - | ns |
| $OE_0$ to any $\overline{Y}$ or Y | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 145 | - | 180 | - | 220 | ns |
| | | | 4.5 | - | - | 29 | - | 36 | - | 44 | ns |
| | | | 6 | - | - | 25 | - | 31 | - | 38 | ns |
| $\overline{OE_1}$ to any $\overline{Y}$ or Y | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 145 | - | 180 | - | 220 | ns |
| | | | 4.5 | - | - | 29 | - | 36 | - | 44 | ns |
| | | | 6 | - | - | 25 | - | 31 | - | 38 | ns |
| LE to any $\overline{Y}$ or Y | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 190 | - | 240 | - | 285 | ns |
| | | | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | | | 6 | - | - | 32 | - | 41 | - | 48 | ns |
| Power Dissipation Capacitance, (Notes 3, 4) | | | | | | | | | | | |
|    CD74HC137 | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 19 | - | - | - | - | - | pF |
|    'HC237 | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 23 | - | - | - | - | - | pF |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | $C_I$ | - | - | - | - | 10 | - | 10 | - | 10 | pF |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay An to any $\overline{Y}$ or Y Address to Output | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 38 | - | 48 | - | 57 | ns |
| | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 15pF | 5 | - | 16 | - | - | - | - | - | ns |
| $OE_0$ to any Y (HC137) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| $OE_0$ to any $\overline{Y}$ (HC237) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 33 | - | 41 | - | 60 | ns |
| $\overline{OE}_1$ to any $\overline{Y}$ (HC137) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 37 | - | 46 | - | 56 | ns |
| $\overline{OE}_1$ to any $\overline{Y}$ (HC237) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| LE to any Y (HC137) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 44 | - | 55 | - | 66 | ns |
| LE to any $\overline{Y}$ (HC237) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 42 | - | 53 | - | 63 | ns |
| Power Dissipation Capacitance, (Notes 3, 4) CD74HC137 | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 19 | - | - | - | - | - | pF |
| 'HC237 | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 23 | - | - | - | - | - | pF |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | | | 15 | | 19 | | 22 | ns |
| Input Capacitance | $C_I$ | - | - | - | - | 10 | - | 10 | - | 10 | pF |

NOTES:

3. $C_{PD}$ is used to determine the dynamic power consumption, per gate.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## *Test Circuits and Waveforms*
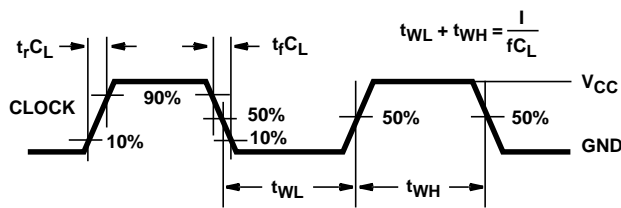
NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**
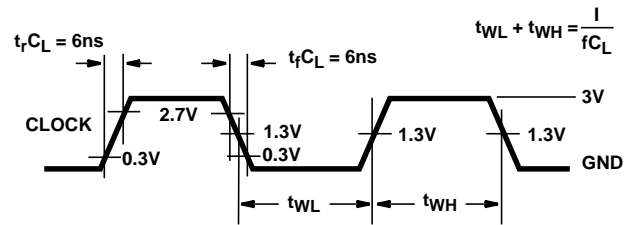
NOTE: Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{MAX}$, input duty cycle = 50%.

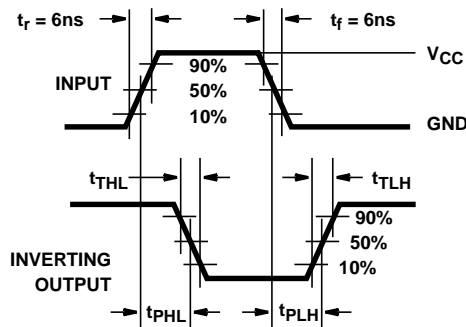**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

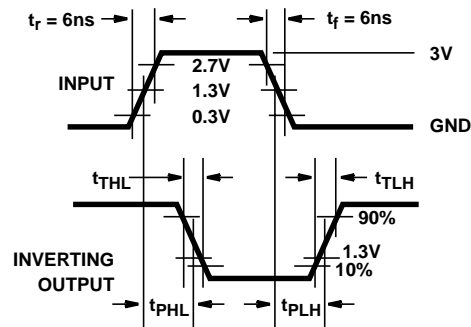**FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**
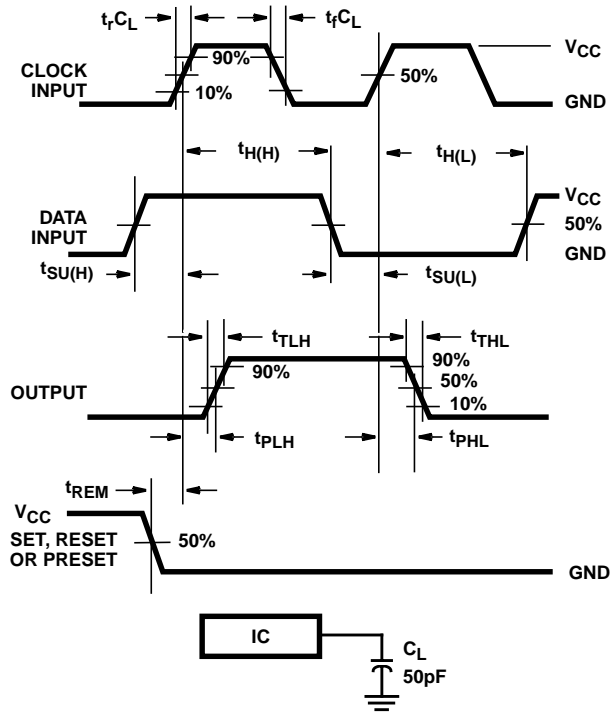
*Test Circuits and Waveforms* (Continued)



**FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**
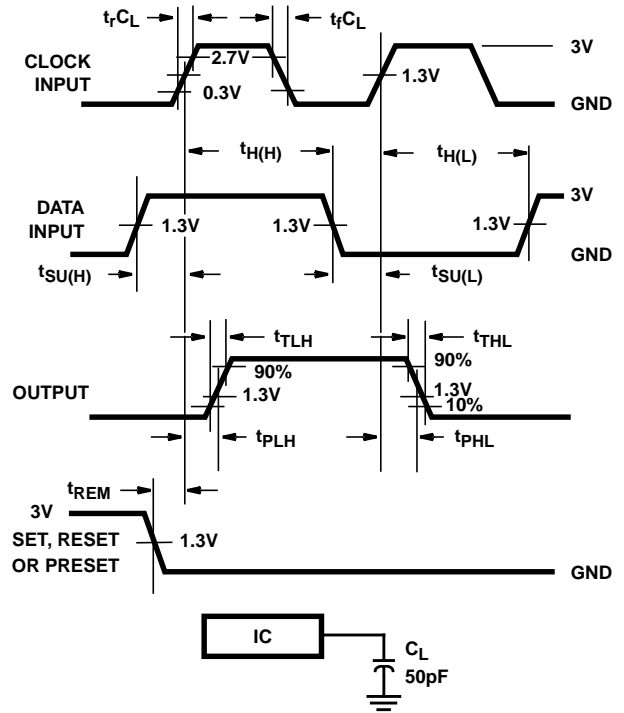
**FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8860601EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8860601EA CD54HC237F3A | Samples |
| CD54HC237F | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD54HC237F | Samples |
| CD54HC237F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8860601EA CD54HC237F3A | Samples |
| CD74HC137E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC137E | Samples |
| CD74HC137PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ137 | Samples |
| CD74HC137PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ137 | Samples |
| CD74HC237E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC237E | Samples |
| CD74HC237EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC237E | Samples |
| CD74HC237M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237MT | ACTIVE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | HC237M | Samples |
| CD74HC237NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC237M | Samples |
| CD74HC237PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ237 | Samples |
| CD74HC237PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ237 | Samples |

# PACKAGE OPTION ADDENDUM

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HCT137E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT137E | Samples |
| CD74HCT137EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT137E | Samples |
| CD74HCT137M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT137M | Samples |
| CD74HCT137MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT137M | Samples |
| CD74HCT137MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT137M | Samples |
| CD74HCT137MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT137M | Samples |
| CD74HCT237E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT237E | Samples |
| CD74HCT237EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT237E | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC237, CD74HC237 :**

● Catalog: CD74HC237

● Military: CD54HC237

NOTE: Qualified Version Definitions:

  ● Catalog - TI's standard catalog product

  ● Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC137PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC237M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC237NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC237PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT137M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC137PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD74HC237M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC237NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD74HC237PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD74HC237PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |
| CD74HCT137M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

0.065 (1,65) / 0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52) / 0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66) / 0.014 (0,36)

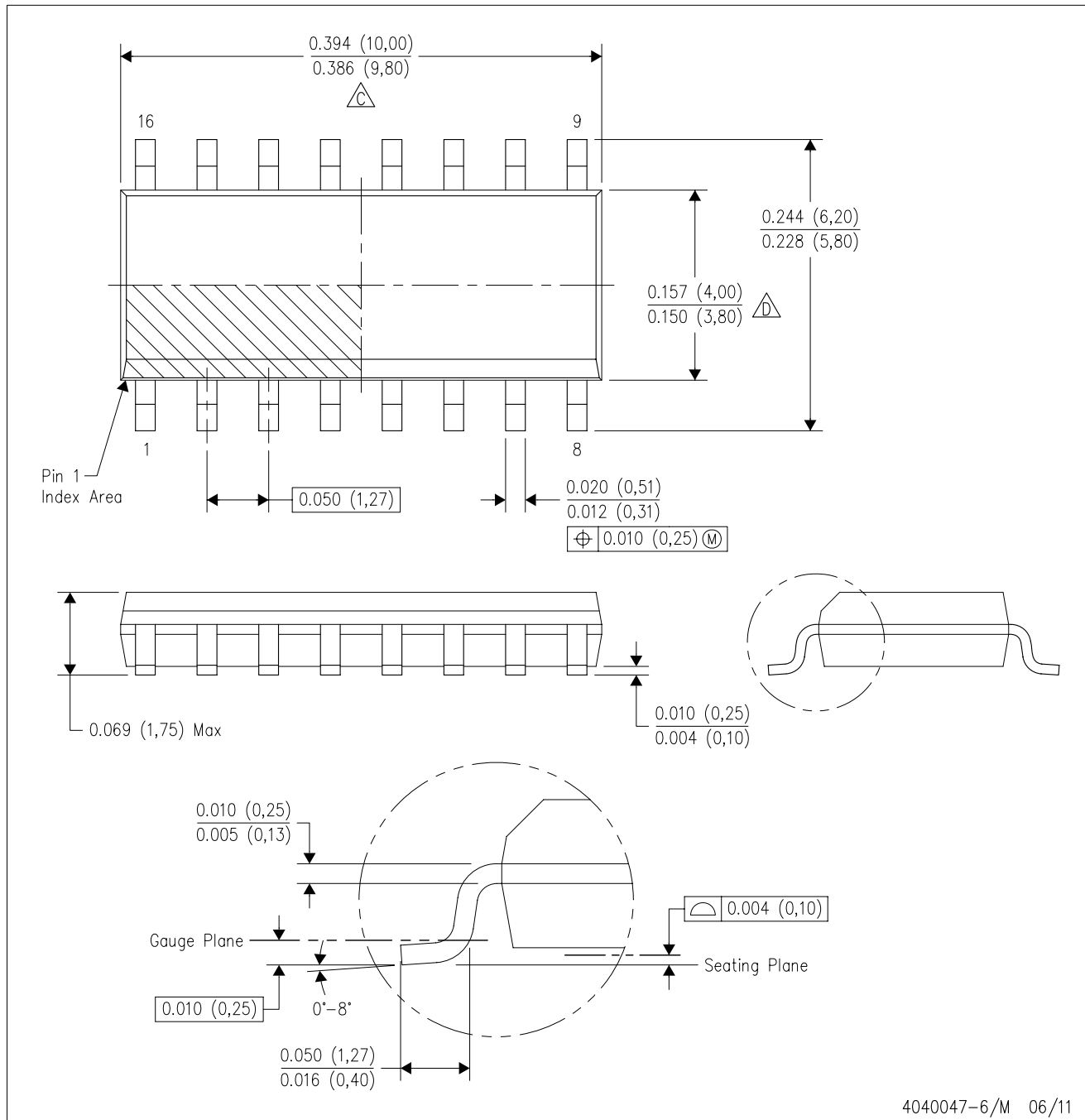0.100 (2,54)

0.014 (0,36) / 0.008 (0,20)

0°-15°

4040083/F 03/03

NOTES:   A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  This package is hermetically sealed with a ceramic lid using glass frit.
          D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.  Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

**N (R–PDIP–T**)**
16 PINS SHOWN

**PLASTIC DUAL–IN–LINE PACKAGE**

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

A

16    9

0.260 (6,60)
0.240 (6,10)

1    8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)
Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

0.010 (0,25) M

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E  12/2002

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G16)                                          PLASTIC SMALL OUTLINE



0.394 (10,00)
0.386 (9,80) △C

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

16          9
1           8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M  06/11

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        △C  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
            not exceed 0.006 (0,15) each side.
        △D  Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
        E.  Reference JEDEC MS−012 variation AC.

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INSTRUMENTS
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D (R−PDSO−G16)                    PLASTIC  SMALL  OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

←16x0,55

←14x1,27

5,40

16x1,50

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,60

1,55

Example
Solder Mask Opening
(See Note E)

←0,07

All Around

4211283−4/E  08/12

NOTES:    A.  All linear dimensions are in millimeters.
          B.  This drawing is subject to change without notice.
          C.  Publication IPC−7351 is recommended for alternate designs.
          D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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INSTRUMENTS
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PW (R−PDSO−G16)                                    PLASTIC SMALL OUTLINE



0,65

0,30
0,19

⊕ | 0,10 Ⓜ

16                    9

Ⓓ  4,50
    4,30

6,60
6,20

1                    8

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50
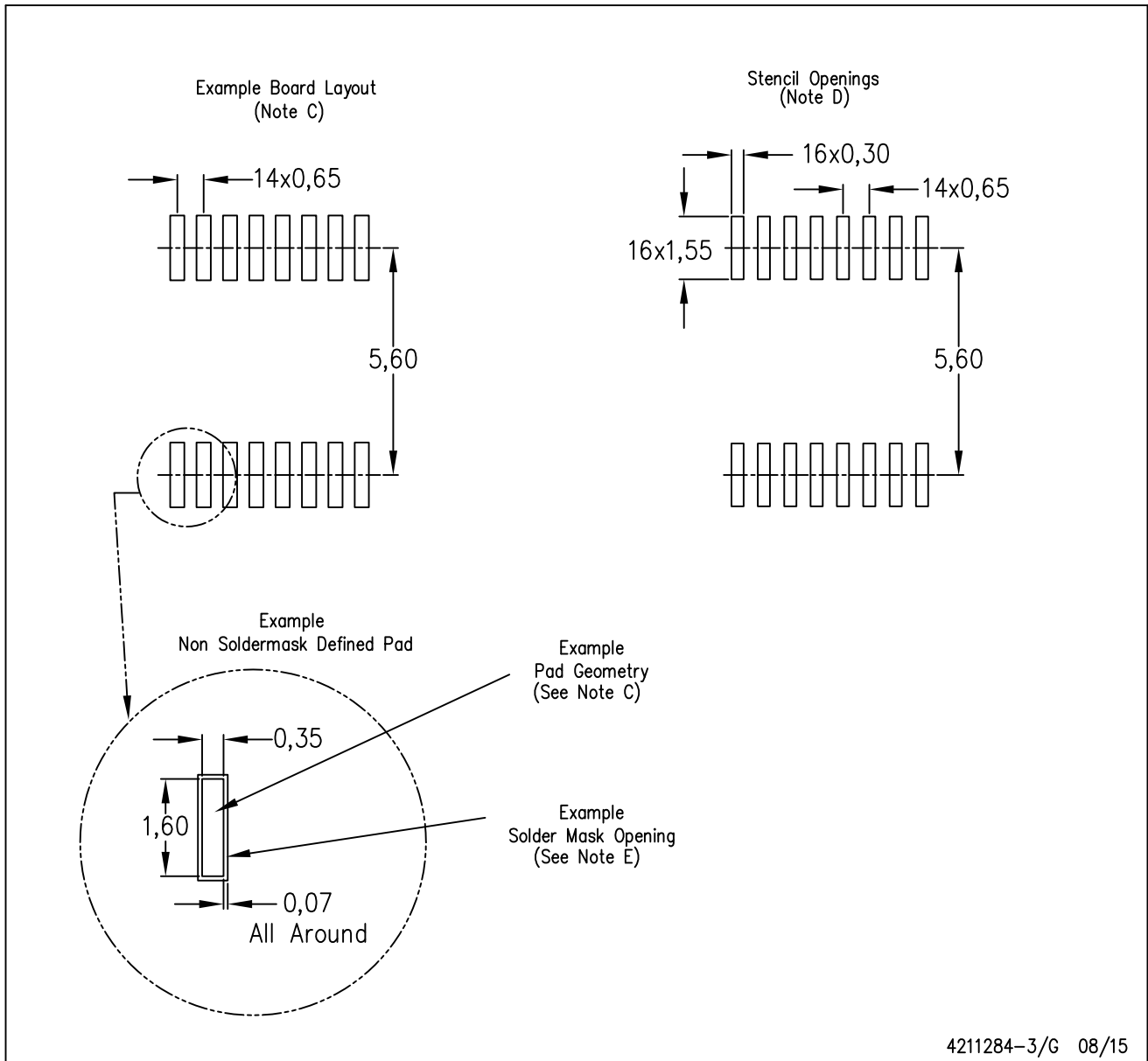
1,20 MAX

0,15
0,05

Seating Plane

◠ | 0,10
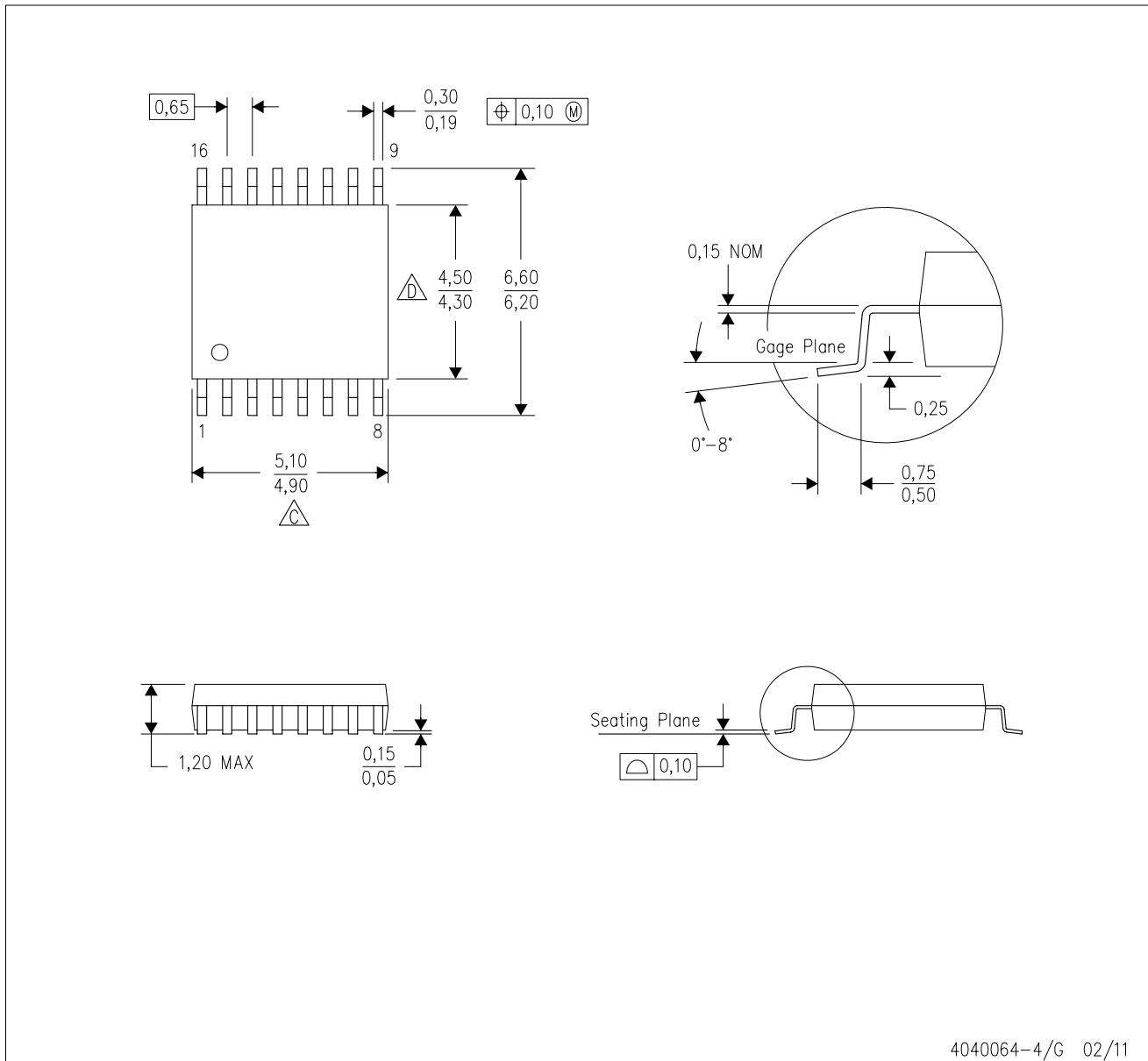
4040064−4/G  02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         Ⓒ   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         Ⓓ   Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

## PW (R-PDSO-G16)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

├─ 14x0,65

5,60

Stencil Openings
(Note D)

├─ 16x0,30

├─ 14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

─ 0,35

1,60

─ 0,07
All Around

4211284-3/G  08/15

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC-7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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NS (R-PDSO-G**)                                                  PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



| | PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|---|
| DIM | | | | | |
| A MAX | | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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